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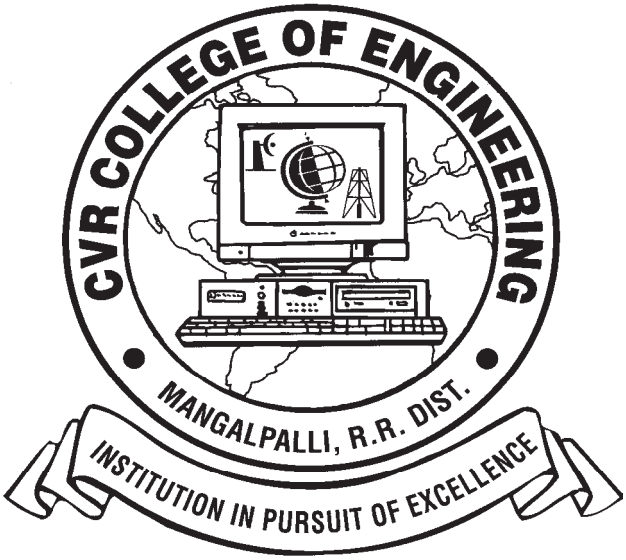

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EDITORIAL

It is with immense pleasure that we bring Volume-10 of the Biannual Journal of our college, CVR Journal of Science and Technology. We have received good number of research papers for review, from our own faculty and from outside our institution. A rigorous filtration process is done, anti plagiarism check by software, and review by experts are done. Finally research papers were selected for publication in the present volume. We are also happy to share with the readers that the college is Accredited by NAAC with 'A' grade and NBA Accreditation is also obtained. Affiliation for all courses and all seats in all branches is also obtained from JNTUH. It is expected that the contributors will further enhance the reputation of the college through this Journal.

The breakup of the papers among various branches is:

ECE – 12, EEE – 2, EIE – 3, IT – 1, H & S – 2

The research papers in the ECE branch cover interesting areas like Emotion Detection by Cepstral Analysis, Sub Threshold source coupled Logic families, low power leakage reduction, spectrum sensing in Cognitive Radio Network etc.

The research papers from EEE Department cover the areas of Hybrid Diesel - Electric propulsion System, Grid Connected Doubly Fed Induction Generator based Wind Turbine. A Survey paper on Routing Protocols in Wireless sensor networks is contributed by I.T. Department. Research papers received from EIE Department cover the areas of Iron Processing with SCADA based Automatic Direct Reduction, Multi-channel UART controller with FIFO and FPGA, sliding mode control of a pH Neutralization system. A study on impact of Green Marketing and Green consumer behaviour is made and this paper is contributed by the Management Science faculty. A paper based on the Novel, "Waiting for Mahatma" is submitted by the English Department.

In the coming issues, all branches of Science, Humanities, Social Sciences and Engineering fields are expected to be covered. Contributors are requested to work on this aspect. The management is supporting the research and Ph.D Programmes, by liberally sanctioning study leave for the faculty. Faculty members working for Ph.D and on research projects are expected to contribute for the journal. Management is also encouraging the authors of research papers with incentives, based on merit.

I am thankful to all the members of the Editorial Board for their help in reviewing and short listing the research papers for inclusion in the current Volume of the journal. I wish to thank Dr. S. Venkateshwarlu, HOD, EEE and Associate Editor, for the pains he has taken in bring out this Volume. Thanks are due to HOD, H&S, Dr. E. Narasimhacharyulu and the staff of English Department for reviewing the papers to see that grammatical and typographical errors are corrected. I am also thankful to Smt. A. Sreedevi, DTP Operator in the Office of Dean Research for the effort put in the preparation of the papers in Camera Ready form.

For more clarity on waveforms, graphs, circuit diagrams and figures, readers are requested to browse the soft copy of the journal, available on the college website www.cvr.ac.in, wherein a link is provided and is available in colour.

Prof. K. Lal Kishore

Editor

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Design of Sub-Threshold Source Coupled Logic Families for Low Power Applications

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***Abstract*--In this paper Standard cell libraries of Sub threshold Source Coupled Logic (STSCL) are developed in 90nm and 45nm technology using cadence virtuoso at 1V power supply. These gates are further used to design digital subsystems like Arithmetic logic unit (ALU) which work at low supply voltages and consume less power with promising performance.**

***Index terms*-- Sub threshold Source Coupled logic, MOS current mode logic, Binary Decision Diagrams.**

I. INTRODUCTION

For mixed signal application, MOS Current mode logic (MCML) or Sub-threshold Source coupled logic (STSCL) have become popular since past decade for high speed and high performance applications. They are a good alternatives for conventional CMOS technologies. Sub-Threshold Source Coupled logic (STSCL) is a good match for low power chips and systems which are used for both technical and business needs like hand held devices [1].

STSCL circuits have reduced switching noise and voltage swing due to its differential nature and immunity to common mode noise and low power dissipation at high frequencies when compared to CMOS STSCL circuits are used in different applications where ultra low power is required because all the transistors in the circuit are operated in sub threshold region and the circuits can operate at very low voltages with constant bias current down to 20p A which is much lesser than CMOS gates.

Reduction of power dissipation may increase the delay of each gate making power dissipation, logic swing and speed being tradeoffs in the design. This paper provides a novel logic families of STSCL which work on differential logic principle with equal and opposite complementary signal outputs with improved noise reduction, less sensitivity to power supply and more freedom for designing the logic gates. Because of these varied advantages STSCL gates have been implemented in many applications like Oscillators, Adders, Multipliers, ADCs, PLL, Microprocessors etc.

II. SUB-THRESHOLD SOURCE COUPLED LOGIC

A. Overview

Any STSCL logic circuit has three main elements: constant current source, source coupled NMOS pairs (pull down network) and the resistive load as shown in figure 1. The logic operation is done in current domain where NMOS switching network is the heart of the circuit which acts as differential pair and decides the logic operation of the gates depending on the arrangement of the these NMOS transistors [2] .It means that here a constant bias current is directed between two output branches which is converted to the output voltage by load resistors.

The speed of switching between differential pair NMOS transistors is very high and is proportional to the bias current of the circuit. In STSCL the load resistors are replaced by PMOS load with the bulk and drain connected as they give high resistance for less tail bias current (bias current) and also occupy less area [3]. This helps STSCL to work in sub threshold region.

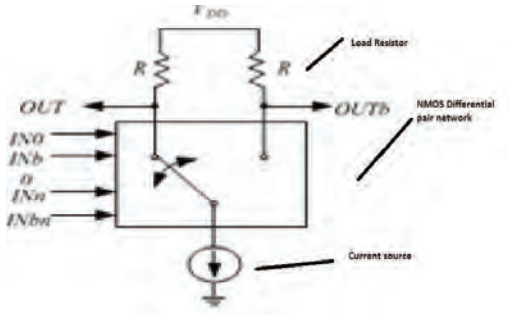

Figure 1 : General topology of STSCL circuit

Thus the output voltage swing V_{swing} of STSCL is decided by the tail bias current I_{SS} and the resistive load R_L.

$$V_{swing} = R_L \times I_{SS}$$

Good voltage swing and tail bias current more than junction leakage current are enough to implement good STSCL circuits with higher load resistances in order of MΩ. The power dissipation of STSCL circuits are constant and does not depend on the clock frequency, it is given by [4]

Power dissipation = V_{DD}. × I_{SS}

The output time constant is given by

$\tau_{SCL} = R_L \times C_L = V_{SW} / I_{SS} \times C_L$

where C_L is total output capacitance.

The power delay product is given by

$PDP_{SCL} = \ln(2) \times V_{DD} \times V_{SW} \times I_{SS} \times C_L$

Thus from above equations it is understood that the delay in the STSCL circuits depends on ISS and not on VDD which is not possible in CMOS topologies, hence the delay can be controlled without influencing PDP. Because of this STSCL can be designed with wide range of bias currents for different speeds and even very low power supplies. STSCL logic gates can work with very low tail bias currents from 10 p A to 100 pA and the power dissipation of these circuits can be reduced to 1fJ/gate which makes STSCL circuits very useful for low voltage-low power applications.

B. Binary Decision Diagrams and STSCL gates

The simple STSCL gate is the inverter/buffer which consists of differential NMOS pair whose sources are connected and given to current source I_{SS} called as tail bias current. The inputs of the STSCL circuit is given to A and its complement $\bar{A}$ applied to NMOS Transistors MN1 and MN2 as shown in figure 2

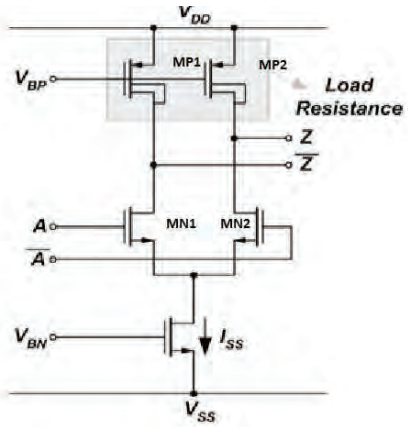

Figure 2 STSCL inverter/buffer

The PMOS transistors MP1 and MP2 act as active loads .The lower and higher digital logic levels are V_{OH}= V_{DD} and V_{OL}=V_{DD}- I_{SS} .R_L .So the logic voltage swing is

$\Delta V = V_{OH} - V_{OL} = I_{SS} . R_D$

After the design of the inverter/buffer circuit, next the basic logic gates like AND/NAND, OR/ NOR XOR/XNOR gates and DFF can be designed by developing a library of cells using the binary decision diagrams (BDD). STSCL logic gates cannot be designed like CMOS logic because STSCL consists of complementary inputs and the output logic level is determined by the switching of the current. BDD use graph algorithms for easy manipulation and have one to one correspondence with STSCL logic networks [5]

In the STSCL circuit, each differential pair represents a node, each interconnection represents an edge and the output nodes represent '0' and '1' leaf nodes of BDD. Thus BDD is directed graph which uses some notations like the result of logic function is shown by the leaf nodes and internal nodes represent one variable, each edge (0 or 1) shows a value assigned to the variable for that particular node from where it is beginning. The graph is a replica of the truth table of the logic gate by going through the path defined by the edges with the weights assigned to their associated variables in that line of the truth table.

For example in the BDD of AND gate as shown in figure 3 and Table 2, consider the combination of A=1 and B=0 the path in BDD results in logic '1'. Like this all the combinations in the truth table are drawn in the graph. The BDD and truth tables of OR gate and XOR gate is shown in figures 4 and 5 below.

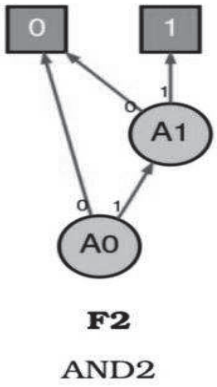

Figure 3 BDD of AND gate

TABLE 1
TRUTH TABLE OF AND GATE

A	B	out
0	0	0
0	1	0
1	0	0
1	1	1

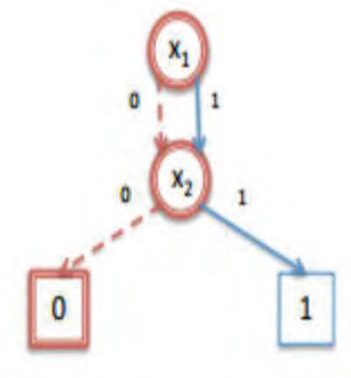

Figure 4 BDD of OR gate

TABLE 2
TRUTH TABLE OF OR GATE

A	B	Output
0	0	0
0	1	1
1	0	1
1	1	1

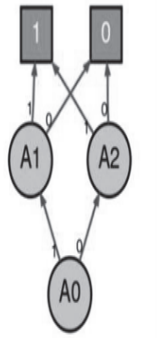

Figure 5 BDD of XOR

TABLE 3
TRUTH TABLE OF XOR GATE

Inputs		Output
A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

III. Implementation And Results

A Circuit Implementation

In this section, different standard cell libraries are designed using STSCL logic to estimate the effectiveness of the proposed STSCL logic [6]. All these logic gates shown in figure 6 are simulated in cadence virtuoso 90nm and 45nm technology and their delay and Power consumption is measured.

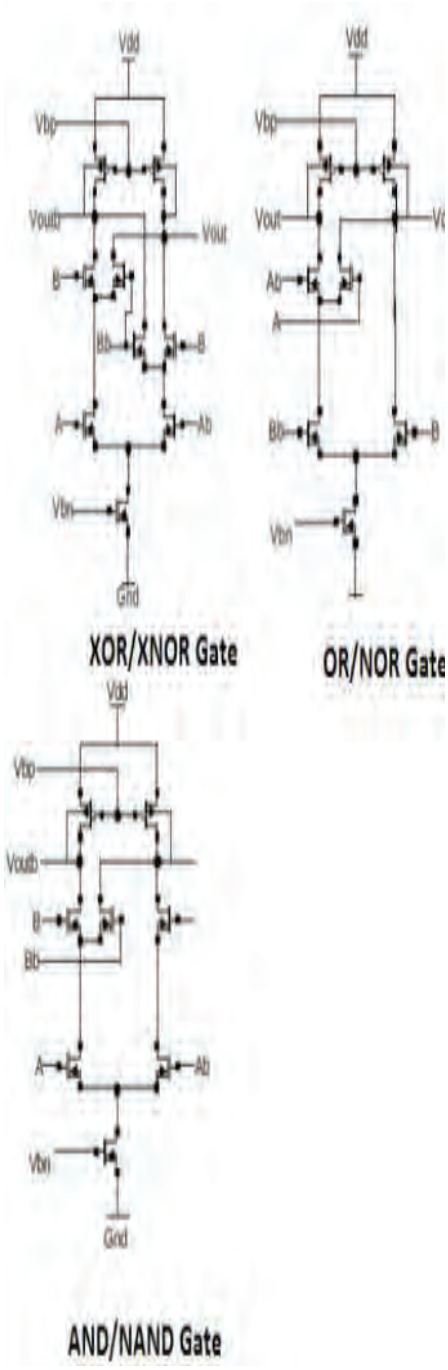

Figure 6 STSCL based XOR/XNOR, OR/NOR, AND/NAND gates

Digital subsystem like 1 bit Arithmetic and logic unit is designed using 8×1 MUX .Full adder and full sub tractor circuits which are designed using STSCL logic and verified as shown in figure 7. For 1 bit ALU conventional

structures are used and the supply voltage for STSCL 45nm CMOS technology for 1 bit ALU design is 1V.

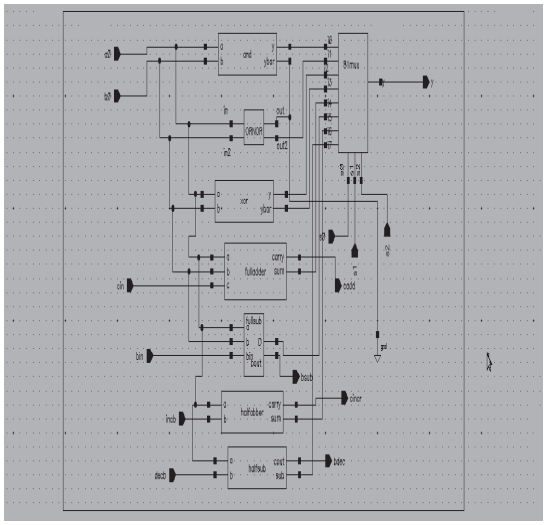

Figure 7 Schematic of 1 Bit ALU

B Results

The simulation results of all STSCL logic gates is given in the figures 8,9,10 below. The simulation results of 1 Bit ALU is given in the figure 11 shown below.

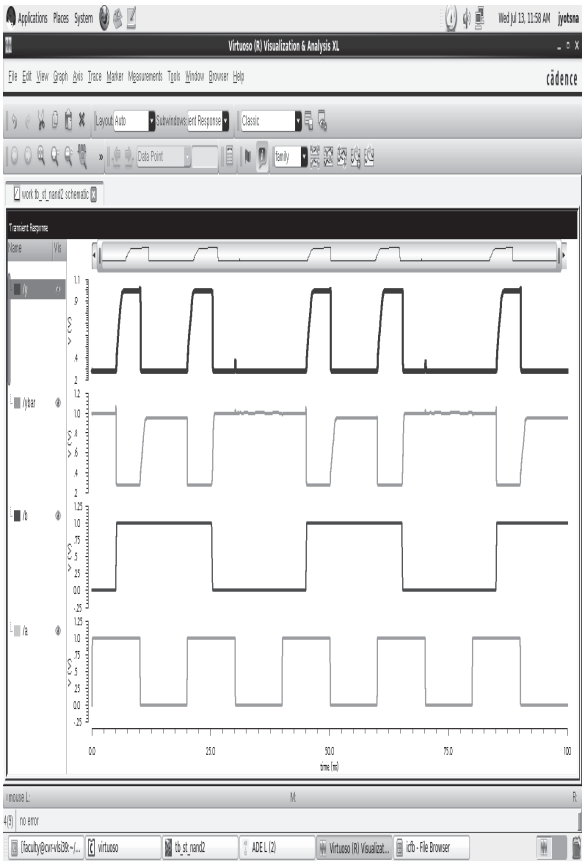

Figure 8 Output of NAND/AND Gate

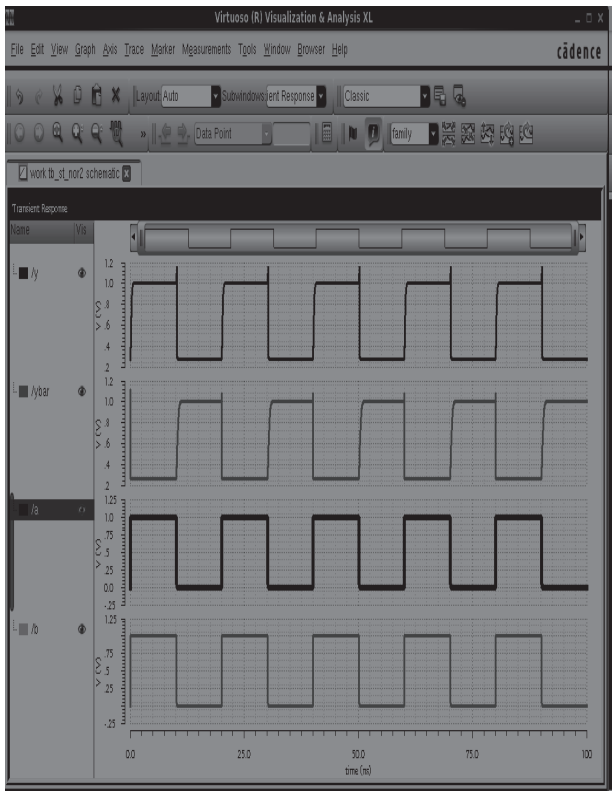

Figure 9 Output of OR/NOR gate

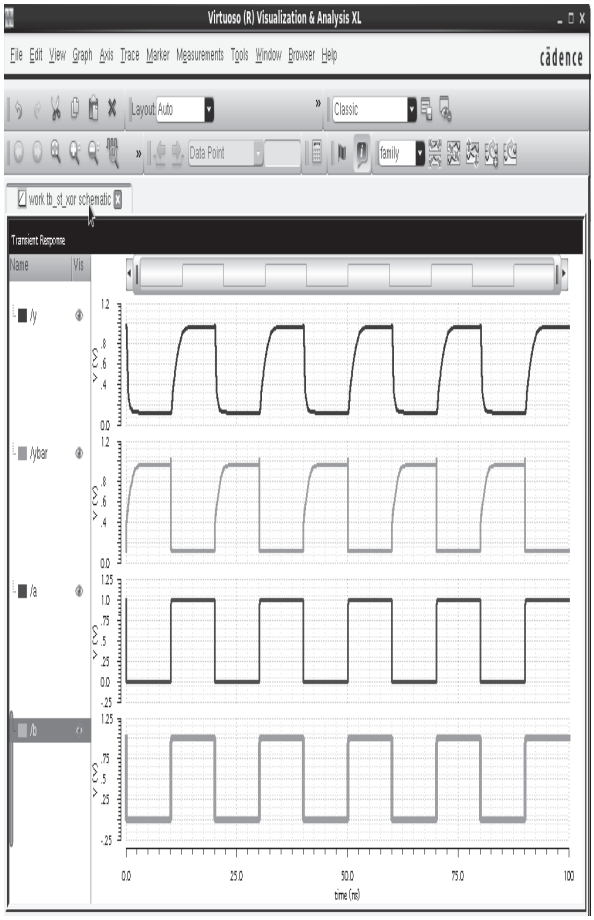

Figure 10 Output of XOR/XNOR Gate

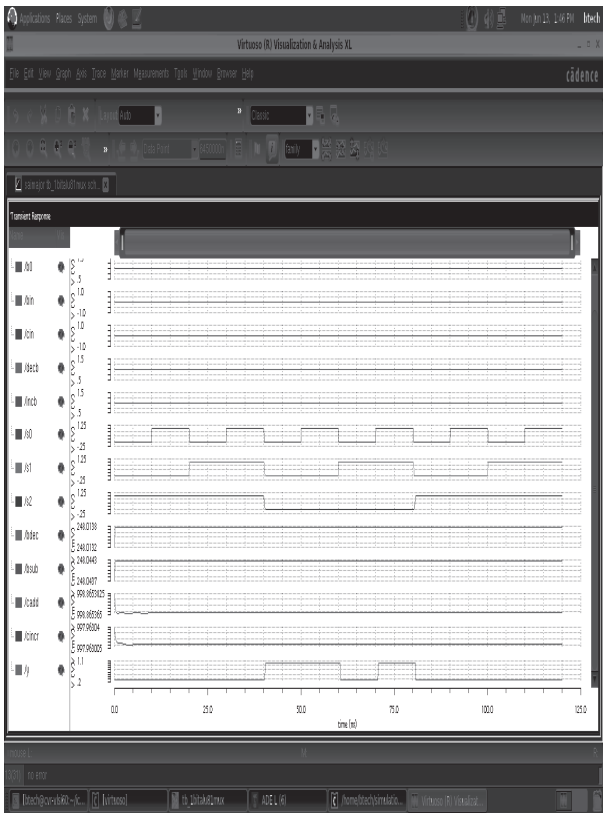

Figure 11 Output of 1 Bit ALU

The power and delay calculations of STSCL logic gates in. 90nm and 45nm technology is compared below in Table 3

TABLE 3

POWER AND DELAY OF BASIC STSCL GATES

Basic Gates	Power and Delay in 45nm		Power and Delay in 90nm	
	Power(W)	Delay(sec)	Power(W)	Delay(sec)
Inverter	7.28E-6	25.32E-12	912.4E-6	1.379E-12
OR	18.76E-6	19 .88E-9	11.1E-6	49.96E-9
AND	22.96E-6	10,04E-9	13.19E-6	30.24E-9
XOR	9.17E-3	20.28E-9	21.9E-6	25.21E-9
NOR	18.76E-6	10.1E-9	11.1E-6	40.0 E-9
N AND	22.9E-6	28.33E-12	27.57E-9	22.57E-9
XNOR	9.17E-3	1 5.24E-9	21.9E-6	126.72E-12

IV. CONCLUSIONS

In this paper a new method of implementing ultra low power STSCL circuits is proposed. Library of STSCL standard cells in 90nm and 45nm CMOS technology is presented and compared. These libraries are used to redesign the existing CMOS digital blocks. This approach benefits from small size PMOS load devices and implements the circuits in nA range. However the area occupied by STSCL circuits is slightly higher because of the differential logic of the circuit. Thus STSCL is a promising alternative to standard CMOS logic for high performance and low power applications.

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Implementation of Emotion Detection by Cepstral Analysis and Noise Filtration in MATLAB

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Abstract— **The main objective of the paper is to determine the emotional state of a person, through his speech. The two most important features that are used to identify the emotional states of a person are i. Pitch and ii. Formant frequencies. To understand the three emotional states of a person, these two pitch and formant frequencies are first extracted from the speech signal and, later their analysis is carried out. The three emotions that are considered are Anger, Neutrality and Happiness. Simulations are carried out in MATLAB and the TU-Berlin database is used for the analysis. For the extraction of pitch frequency Cepstral analysis method is used and the formant frequencies are estimated to detect happy emotions. The objective of cepstral analysis is to separate the speech into its source and system components without any prior knowledge about source and / or system. This separation is done due to difference in occupancy of frequency ranges. Following it, noise filtration is implemented to remove inaudible ambient noises.**

Index Terms— **cepstral analysis, emotion, filtering, formant frequencies, noise**

I. INTRODUCTION

In the present era of modernization, comes the need of automation. Many of the things around us tend to be controlled automatically. Once the word 'automatic' is being used, a person's speech/voice plays an important role. Processing of one's speech signal and extracting some features of the speech is known as speech signal processing. Speech signal processing [1] has its applications in various areas like speech coding, speech recognition, speaker recognition, speech enhancement, emotion detection etc. Study on speech signals has developed very much in the recent past due to various sophisticated algorithms being developed like vector quantization, hidden Markov model, cepstral analysis etc. In this paper, cepstral analysis is used to extract the pitch and formant frequencies from the speech signal to identify the emotional states of a person.

The paper is organized as follows. Section II covers the basic principles of cepstral analysis. The proposed work is described in section III. Simulations are carried out using MATLAB. Section IV gives the results and section V gives conclusions.

II. CEPSTRAL ANALYSIS

Considering the source-filter theory, the production of speech can be categorized into two stages. The first stage involves generation of a sound source which has its own spectral shape and spectral fine structure. In the second stage the sound source is then shaped or filtered by the resonant properties of the vocal tract. According to signal processing, speech can be considered as the output coming from a system (i.e., entire vocal tract) which is excited by an input (i.e., vibration of vocal folds). The separation of these two i.e., deconvolving them is necessary to process the speech.

If there is prior knowledge about the input excitation, then it is possible to separate the system component and construct it by exciting the system with the input and finally collecting its responses. If there is knowledge about the response of the system, then it is possible to recover input excitation by using the concept of inverse filter theory. The excitation is recovered using Linear Prediction analysis of speech. There is another method of deconvolution wherein the assumptions are input excitations and which has unknown system responses. The proposed work is based on this type where the responses and the input excitations of the system are not known.

Speech is composed of excitation source and vocal tract system components. In order to analyze and model the excitation and system components of the speech independently and also use that in various speech processing applications, these two components have to be separated from the speech. The objective of *cepstral analysis* is to separate the speech into its source and system components without any prior knowledge about source and / or system.

If the excitation sequence is e(x) and the vocal tract filter sequence is s(x) then the speech sequence h(n) can be written as

$$s(x)=e(x)*h(x) \quad (1)$$

In frequency domain this can be written as

$$S(w)=E(w).H(w) \quad (2)$$

The above equation (2) conveys that the multiplication of excitation and system components in the frequency domain gives the convolved sequence of the same in the time domain. The deconvolution involves the speech to be deconvolved into the excitation and the vocal tract in the time domain. Thus, cepstral analysis is carried out for transforming the multiplied source and system components in the frequency domain to linear combination of the two components in the cepstral domain.

From the Eqn. (2) the magnitude spectrum of given speech sequence can be represented as,

$$\left|S\left(w\right)\right|=\left|E\left(w\right)\right|\left|H\left(w\right)\right| \quad (3)$$

To linearly combine the E(ω) and H(ω) in the frequency domain, logarithmic representation is used. So the logarithmic representation of Eqn. (3) will be,

$$\log\left|S\left(w\right)\right|=log\left|E\left(w\right)\right|+\log\left|H\left(w\right)\right| \quad (4)$$

In the above equation (4), the logarithmic operation is used which transforms the magnitude of the speech spectrum. Here the excitation component and the vocal tract component are multiplied. By using this logarithmic operation, multiplication of components is converted into summation components in the frequency domain. By using the inverse discrete fourier transform (IDFT) the separation of excitation and vocal tract system components is done. IDFT of linear spectra transforms back to the time domain but the IDFT of log spectra transforms to quefrency domain or the cepstral domain which is similar to time domain. The following equation (5) gives the mathematical concept of IDFT. In cepstral domain, the vocal tract component representation is shown as slowly varying components concentrated near the low quefrency region and excitation components by fast varying components at higher quefrency region.

$$\begin{aligned} &log\left(E\left(w\right)+log\left|H\left(w\right)\right|\right) \\ &c\left(n\right)=IDFT\left(log\left|S\left(w\right)\right|\right)=IDFT \end{aligned} \quad (5)$$

Reason for higher order coefficients representing excitation characteristics:

Voice signal basically involves periodic impulse sequences impinging on the vocal tracts, i.e. a train of impulse is the excitation repeating at periodic intervals say τ

$$x(t) = s(t)+\alpha s(t-\tau) \quad (6)$$

The Fourier spectral density (spectrum) of such a signal is given by

$$|X(f)|2 = |S(f)|2[1+\alpha 2 +2\alpha\cos(2\pi f \tau)] \quad (7)$$

Thus, from (7) it is clear that the spectral density of a signal with an echo has the form of an envelope (the spectrum of the original signal) that modulates a periodic function of frequency (the spectrum contribution of the echo).

Hence after every few samples pertaining to τ time interval, one can observe a peak in spectrum which is due to the train of impulses. Hence the upper quefrequency samples represent the excitation characteristics.

III. PROPOSED WORK

A. Pitch and Formants

Pitch [2] is the frequency at which one can observe maximum amplitude of vibration of vocal folds. It is also the fundamental frequency of the vibration. As per the above theory it's clear that vocal fold characteristics can be observed from higher order coefficients say after 20 samples of cepstrum.

A formant can be defined as a concentration of acoustic energy around a particular frequency in the speech wave. Since they represent the filter (chords) characteristics, these frequencies can be obtained from the lower quefrency components of cepstrum.

The work is carried out by first implementing a noise filter to remove low frequency ambient noise. This filter code is then used in emotion detection to filter ambient noises while recording live speech samples giving provision for live testing apart from recorded samples. The code first calculates the pitch of the signal and then the formants. Pitch has been used for identifying angry emotion, whereas formants are used to identify happiness [3].

The TU_BERLIN (Technical University of Berlin) database has been used to get recorded samples. The database consists of samples of voice spoken by professional actors with various sentences and emotions. These samples and the samples from movie clips had been used to test and identify the pitch and formant ranges of the emotions based on which the code had been written.

A low pass butterworth filter had been used to remove noise. The order of the filter can be increased or decreased based on type of noise to be removed. The code removes ambient noise and car horn noise. A 10^{th} order filter had been used for car horn sound removal.

B. Pitch : Used to detect anger

Vocal folds vibrate at a very faster rate when a person is angry, thus making the interval τ very small and thereby increases the pitch of the speech. It has been observed that the pitch of neutral speech is much less when compared to the pitch of angry speech. Hence the pitch of the speech is considered to detect the emotion anger [4] [5].

Table I. below gives the pitch frequencies for six different speakers, each in various languages like one in English, three in Telugu and two in German when the

emotional state is anger. Table II. gives the pitch frequencies of four speakers in German, Telugu and English in neutral state. It is found that the frequency range for neutral state is less as compared to that of anger state. Also the pitch frequencies [6] lie in approximately the same range of frequencies when the emotional state is anger, irrespective of the languages used and the speakers. Pitch frequencies for neutral and anger emotion states are found to occur at approximately 300Hz and 200Hz respectively.

TABLE I.
OBSERVATIONS FOR HAPPY EMOTIONS

Number of Speakers	Language	F1	F2	F3
Speaker 1	German	363	915	1800
Speaker 2	Telugu	432	979	2267
Speaker 3	Telugu	419	819	1253
Speaker 4	Telugu	296	671	1195
Mean		**377**	**846**	**1629**

TABLE II
OBSERVATIONS FOR NEUTRAL EMOTIONS

Number of Speakers	Language	Pitch Frequency
Speaker 1	German	230
Speaker 2	German	139.13
Speaker 3	Telugu	189.04
Speaker 4	English	216.216
Mean Frequency		**193.6**

C. Formant: Used to detect happiness

Since they represent the filter (chords) characteristics, these frequencies can be obtained from the lower quefrecny components of cepstrum. The fundamental frequency (pitch) when the emotion is happy is less. Under such conditions the formants coincide with the spectral peaks of the filter coefficients. Hence, taking the FFT of the lower quefrency samples and finding spectral peaks gives the formant frequencies enabling us to detect the happy emotion [7].

Table III. below gives the observations for happy emotions. Here formant frequencies are extracted and three different frequencies f1, f2 and f3 are used to detect the emotional state. The analysis is performed on four different speakers, first speaker being German and remaining three are Telugu. The mean values are also calculated and it is found that the formant frequencies occur at three different bands. F1 occurs at around 300Hz, f2 at around 800Hz and f3 at 1600 Hz.

Pitch and formant frequencies are both calculated for every sample. It is observed that pitch of angry samples is different from pitch of neutral and formants of angry and happy are also different.

IV. RESULTS

A. Plots of Noise Filtration

Normalized plot of the spectrum brings in all the frequency components within range of [0 ,1] samples, considering only a half plot of the spectrum. Figure 1 clearly shows the noise part of the signal at higher samples.

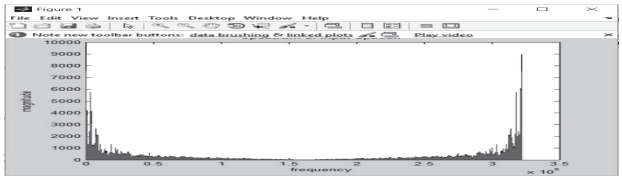

Figure 1. Spectrum of Input Speech Signal

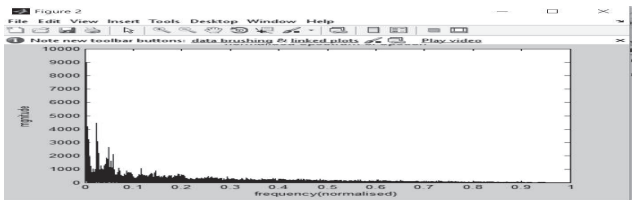

Figure 2. Normalized Spectrum of Input

Since a Low Pass Filter is used, all the higher frequency range values of the spectrum are removed. Figure 3 clearly depicts the removal of noise.

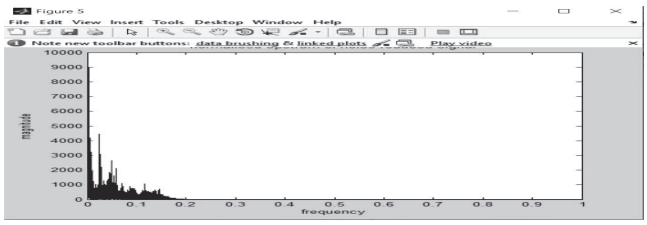

Figure 3. Filtered Output Spectrum

Cepstral analysis is applied on a 20ms speech sample. Considering the sampling frequency of 8000Hz, a 20 ms duration of speech signal has 160 samples to which cepstral analysis has been applied. Figure 4 shows the details of the cepstrum of the speech. Pitch can be identified by observing the peak after 20th sample till 80th sample.

B. Plots of Cepstral Analysis

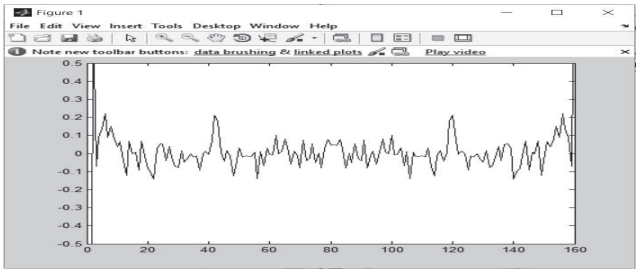

Figure 4. Cepstrum

Formants, as mentioned, are calculated by applying Fourier transform to lower samples of cepstrum. The peaks coincide with the formants. Figure 5 shows the formants as * mark in the spectrum.

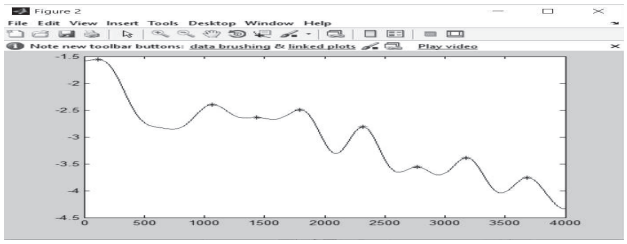

Figure 5. Formants

V. CONCLUSIONS

It is clearly seen that cepstral method of analysis of speech is one of the best speech processing techniques developed for various applications. It was originally invented for characterizing the seismic echoes resulting from earthquakes and bomb explosions. But later it has proved to be an efficient method to evaluate human vocal tract characteristics (formants) and pitch of the speech signal. This was made possible due to application of logarithm which enabled separation of source and system components of speech (as per source-filter speech theory). Also these characteristics of pitch and formants are observed to be unique for different emotions like anger and happiness and hence, available to detect the emotion of a person through his speech with good accuracy. It is also observed that the emotional states of a person appear over a range of frequency bands. In this paper three emotions states i.e., angry, neutral and happy are recognized by finding the pitch and formant frequencies. For angry and neutral state, the pitch frequencies are centered around 300Hz and 200Hz respectively whereas for happy state the formant frequencies are centered at around 300Hz, 800Hz and 1600Hz.

The present consideration of emotion detection can be completely used to involve other states of emotion like sadness, boredom etc. with the involvement of image processing to observe the facial expressions of the individual, thus improving the accuracy.

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Design of Fast Locking ADPLL via FFC Technique using VHDL-AMS

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***Abstract*—In this paper ADPLL is designed via feed forward compensation technique and implemented using VHDL mixed signal Modeling technique in CADENCE. The use of mixed signal is that it can simulate SPICE codes, VHDL codes, Verilog codes and Verilog –A codes at a time using both SPICE simulator and Incisive Unified Simulator. The ADPLL consists of PFD, P2D, FDLPF, MD, LC and DCO blocks.The PFD block was designed using transistors. The FDLPF, LC and DCO blocks were designed using VHDL. The MD and P2D blocks were designed both by using VHDL and transistors. The implemented ADPLL achieves a fast frequency locking via the proposed feed-forward compensation algorithm, reduces power consumption and wide tunable frequency range.The designed ADPLL is very much suitable for SOC applications.**

***Index Terms*—All Digital Phase Locked Loop, Phase Locked Loop, Analog and Mixed Signal, System on chip**

I. INTRODUCTION

The PLL is a very important and common part of high performance microprocessors. These are widely used in clock generators for SOC microprocessors. In general, a PLL is made to work as an analog building block, but it is difficult to integrate an analog PLL on a digital chip. Therefore, the implementation of the loop filter and oscillator circuits in PLLs became popular.This type of PLL is called as All-Digital Phase Lock Loop [1].

Analog PLLs are more unsteady to noise and process variations. Digital PLLs allow a faster clock time. In high performance microprocessors, clock generation is achieved from digital PLLS[2].

ADPLL is a phase lock loop implemented in simple digital circuitry. It operates on finite precision digital words.The general ADPLL consists of four blocks. They are Loop fliter, Phase detector, Numerically controlled oscillator and Free running phase blcok as shown in the Figure 1.

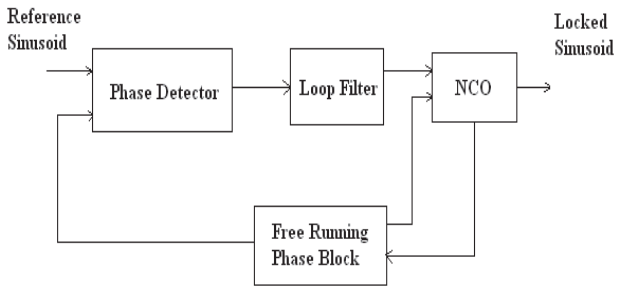

Figure 1. General ADPLL

The phase detector gives data about the difference in-phase and its two input signals. Digital multiplier creates a DC signal using reference signal. The created DC signal is proportional to the phase difference and a series of higher frequency components. The high-frequency terms which are created through multiplier are stored in the phase detector. The loop filter filters the stored data of the phase detector. The loop filter is usually a first or second order infinite impulse response (IIR) low-pass filter. The output of filter is passed through numerically controlled oscillator (NCO). The function of NCO is to adjust phase and frequency, by reducing the phase error to zero. This condition is called as phase lock. The frequency of the reference signal is within a defined distance from the free-running or open loop frequency of the NCO, known as pull-in range[2]. Frequency deviation between the two signals before they unlock is defined as hold range. Pull-in time is defined as the time taken to lock the loop. These parameters can be controlled by modifying the loop bandwidth of the ADPLL, but it cannot achieve good response only with these blocks. So, a new technique called feed forward compensation technique is implemented.

To improve the dynamic response of ADPLL Feed forward compensation is used successfully in many control systems. In PLL system design, the channel-switching event is disturbance from the point of view of controlled system. Since the disturbance is known, it is used to improve system performance.The block diagram of feed forward compensation is technique shown in the Figure 2.

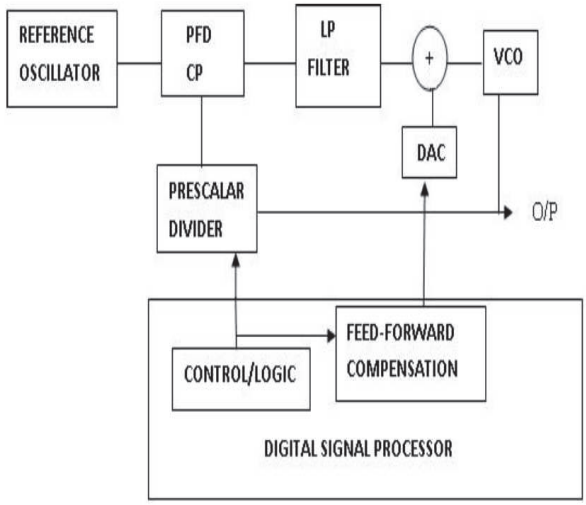

Figure 2. Feed Forward Compensation Technique

In different divider ratio, dynamic response is made by the constant loop gain. This is done by multiplying the original loop gain with the known divider ratio.This data is used directly to adjust the VCO control voltage. The channel selection command from the DSP chip determines the divider ratio N. The desired VCO control signal is determined by a feed-forward controller. The converted VCO control signal from the analog domain is added to the feedback control signal.

In addition to the feed-forward control signal, feedback is necessary for feedback loop because of its unreliability result of VCO modelling error, DSP algorithm errors, DAC error, etc. The feedback loop is also used for reduction of close-in VCO phase noise, since the loop has a narrow bandwidth.

In this method, feed-forward controller decides the VCO control signal through the major component. The dynamic behaviour of the whole system has a comparatively small effect than the feedback loop. Change of loop gain by change of divider ratio will not affect the switching speed.

II. ARCHITECTURE OF EXISTING ADPLL

The architecture of existing All-Digital Phase Lock Loop by using FFC technique is shown in Figure 3. It consists of a phase/ frequency detector (PFD), a Modified Divider (MD), a Loop Control (LC), a ring type Digital Control Oscillator (DCO), a First-order Digital Loop Filter (FFDLPF), and a Phase to Digital converter (P2D). Here the existing ADPLL DCO has five clocks whose phases are different. The five clocks are named as CLK [0], CLK [1], CLK [2], CLK [3] and CLK [4]. CLK [1], CLK [2], CLK [3] and CLK [4] are written as for short CLK [4:1].

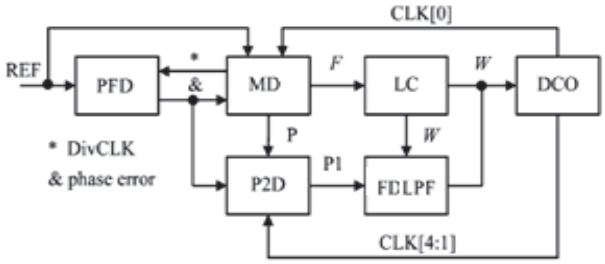

Figure 3. Architecture of Existing ADPLL with FFC

The designed blocks are connected in both feed forward and feed backward directions for the frequency acquisition mode and phase acquisition modes respectively. Here the reference clock is given by the user and the other clocks generated by the ring type DCO. Later these clocks are joined on the MD block to get the phase error and fed into the P2D to digitize the phase error. Here in existing ADPLL except LC all blocks are designed using transistors. Each block explanation is given below.

A. Design of PFD

The Phase frequency detector plays a significant role in PLL because it detects a difference in phase and frequency between the reference and feedback signal. The PFD output depends on both the inputs of phase and frequency. The design uses two flip-flops with reset features along with one AND gate, one OR gate and one Exclusive-OR gate.

The two D-inputs of flip-flops are connected to VDD. The two clock inputs of flip-flops are connected to Reference clock and Divide clock respectively. The output of flip-flops are Up and Down signals respectively. If the reference signal falls first, then up signal goes to high-level and down signal goes to low-level and if divide signal falls first, then down signal goes to high-level and up signal goes to low-level. If both the signals are at high-levels, then the two signals reset to low-levels of a feedback reset signal.

In the feedback loop output of AND gate is given to one of the OR gate input. The other input of the OR gate is, named as reset_div, and if it is, set of high-level, then the two D flip-flops in the PFD resets. The up and down signals are connected to a Xor gate to get the phase error signal as the output.The schematic design of PFD is shown in the Figure 4. Here the designed D-Flip-flops use transmission gates.

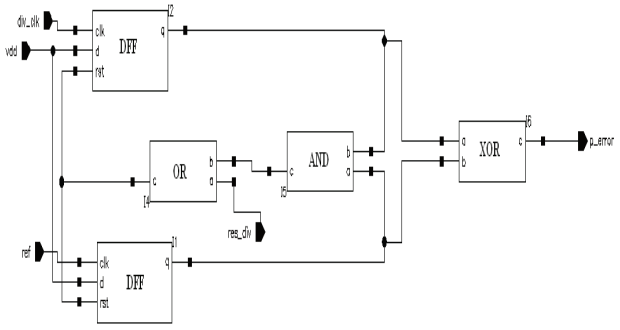

Figure 4. Schematic of PFD

B. Design of MD

It is the modified form of asynchronous frequency divider. Generally DIV used to generate the divider clock at high frequencies using DCO clock. In the modified DIV along with divider extra three modules were added. They are saveF module, Reset_syn module and T2D module.

The function of saveF module is to store the data according to the reference signals. It has two reference signals. One reference signal saves the value of the counter in the divider block and the other reference signal is used to store the counter value in the register block. Both the signals use raising condition. This module has a D-Flipflop and a register.

The function of the Reset_syn module is to readjust signals, to control operation of the divider. When the reset signal is at low-level, then the divider counts by the rising-edge of the clock and when it is at a low-level then the counter gets reset for the next counting operation and leaves the time for LC to tune DCO. This module consists of D Flip-flops, AND gate and OR gate.

The function of T2D module is to convert the phase eror to digital formats. It consists of a D Flip-Flop, two Registers and two adders. Here the sensed phase error by

the PFD is re-sampled on the falling edge of the clock and the value is stored in the registers during the rising edge of the signal phases because of the adoption of the feed-forward compensation algorithm. The schematic design of the MD is shown in the Figure 5. Here all the designed blocks use transistors.

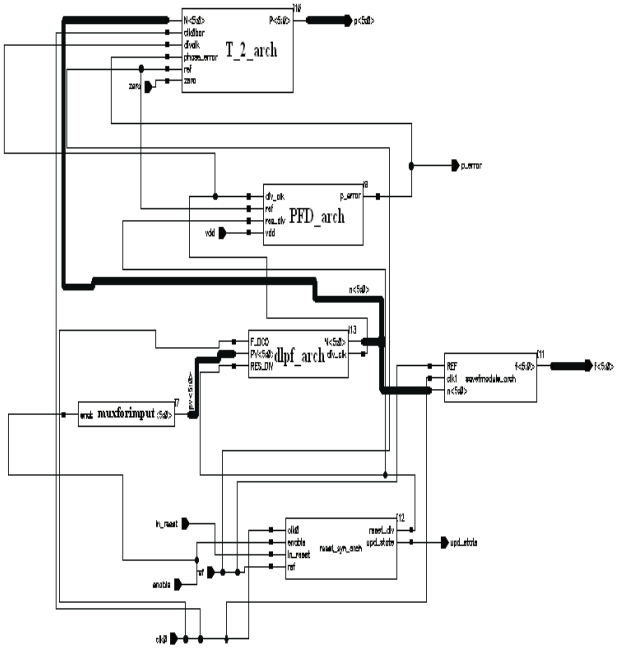

Figure 5. Schematic of Modified DIV

C. Design of LC

Loop Control is a digital processing section and when the ADPLL is initialized it performs two operations. First, the LC calculates Kf parameter coming from MD and second it generates W locked signal. The generated W locked signal is given to FDLPF and DCO.This block consists of four adders, one multiplier and one divider.

Two reference cycles are needed to obtain the parameter Kf, from the algortihm. The values of F1 and W1 are obtained from the first reference clock. The values of F2 and W2 are obtained from the 38 reference cycle. By division operation, Kf value is calculated. The dividend is ΔW=W1–W2 and the divisor is ΔF=F1–F2. The LC predicts the code W from the obtained Kf. The divider is used to divide A and B values that mean ΔW divided by ΔF [1]. Here VHDL codes are written for all the blocks. The symbol generation of LC using VHDL is shown in the Figure 6.

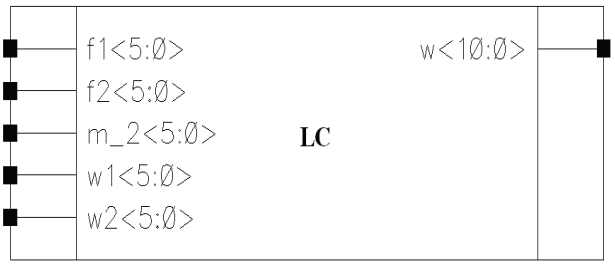

Figure 6: Symbol generation of LC

D. Design of DCO

The Digital controlled oscillator consists of both digital-to-analog converter and a Voltage controlled oscillator. The DAC changes input to the voltage Vc based on the input code. The changed voltage Vc controls the frequency of the voltage controlled oscillator. The DCO design includes a delay cell and voltage controlled cell for the conversion and controlling of frequency. The designed delay cell consists of two inverters and a modified NOR cell. The output of the delay cell will be at low-level when the input run signal turns to high-level during off state of the PLL. Due to this condition the power reduces. The voltage Vc controls the frequency of the VCO, when the signal run is at low-level. If the voltage Vc increases the delay time, then delay cell time decreases and the frequency of the VCO increases. The schematic design of the DCO cell is shown in Figure 7. Here all the blocks are designed using transistors.

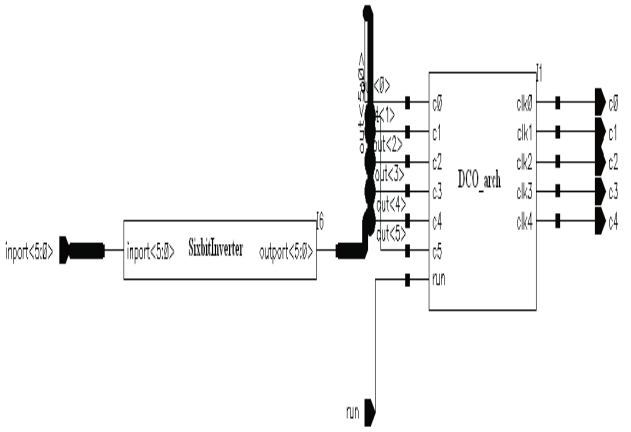

Figure 7. Schematic of DCO

E. Design of FDLPF

This is a First order digital loop filter and consists of two parameters. It consists of two adders, one multiplexer and one inverse block. It gets a W locked signal from LC and phase error signal p1 from P2D as the inputs. When the select signal of the multiplexer is set to high-level, then the code predicted by the LC is inserted into the integral path. The output of the FDLPF block is fed to the input of the DCO. The schematic design of FDLPF is shown in Figure 8. Here all the designed blocks use transistors.

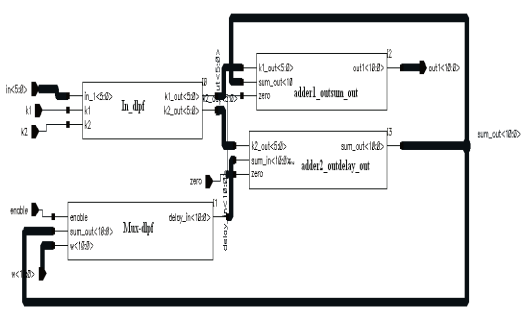

Figure 8. Schematic of FDLPF

F. Design of P2D

The P2D is used to reduce the quantization error of the MD. This is possible only by adding the four DCO clocks through counter process. The design consists of four 2-bit counters, four comparators, one multiplier and two adders. The detected phase error of MD is connected to the P2D for its observation.

The generated clocks from DCO are connected to four clocks for triggering the counter. The two lowest LSB's of the counter are compared by four comparators which are connected to the output of the counter. Compared result is then multiplied by 5 and added to the sum of the comparison results and then forwarded to the FDLPF. The schematic design of P2D is shown in the Figure 9. Transistors are used for designing entire blocks.

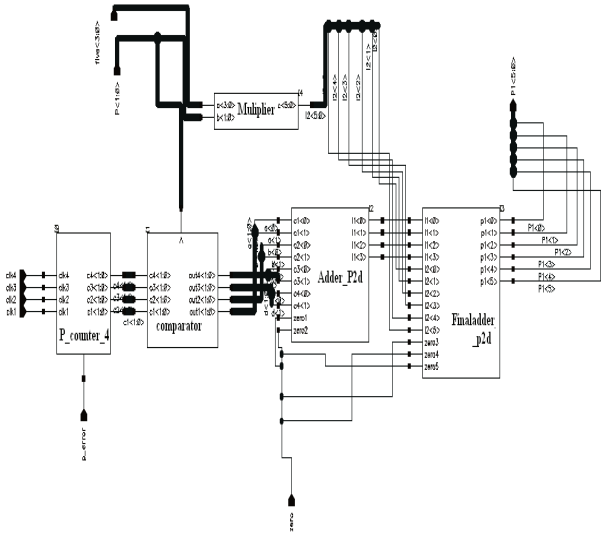

Figure 9. Schematic of P2D

III PROPOSED ADPLL

In Proposed ADPLL, both transistors and VHDL are used for designing MD and P2D blocks.VHDL is only used for designing FDLPF and DCO blocks. The PDF design is also included inside the MD block. The schematic of the proposed ADPLL design is shown in the Figure 10.

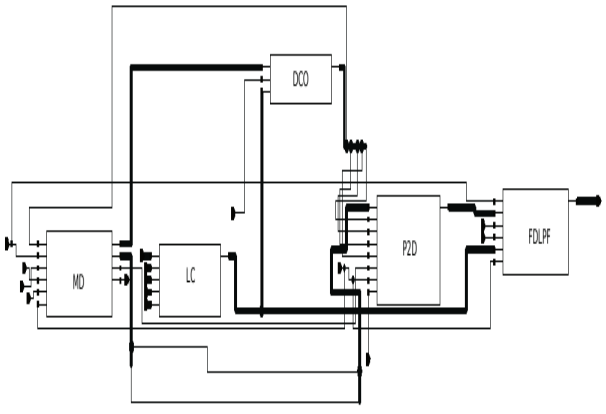

Figure 10.Schematic of proposed ADPLL

A. Design of MD

The MD designed here consists of T2D module, PFD module, SaveF module, Reset_syn module, Divider module and a multiplexer for input divider. Here VHDL codes were used for designing T2D module, Divder module and multiplexer for input divider modules. Flip-flops and registers are used for designing PFD and SaveF module which in turn uses CMOS transistors. The symbol generation of MD using VHDL and transistors is shown in the Figure 11.

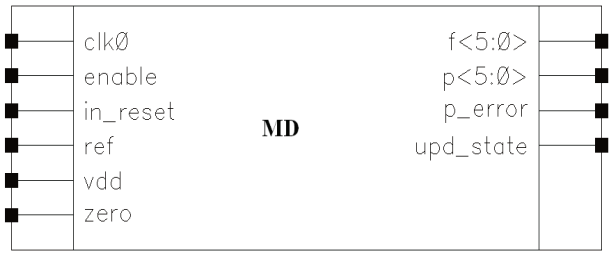

Figure 11. Symbol generation of MD

B. Design of P2D

The P2D designed here consists of one multiplier, four bit-counter, four bit-comparator and two types of adders. Here VHDL is used for designing multiplier, four bit-counter and four bit-comparator. The two types of adders were designed using half-adder, full-adder and flip-flops which are intern designed using gates. The symbol generation of P2D using VHDL and transistors is shown in the Figure 12.

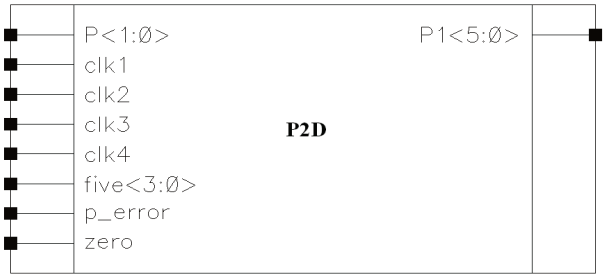

Figure 12. Symbol generation of P2D

C. Design of FDLPF

The FDLPF designed here consists of two types of adders, one multiplexer and one inverse block. Here one adder generates the sum and the other one used to generate output delay. Here all the blocks are designed using VHDL. The symbol generation of FDLPF using VHDL is shown in Figure 13.

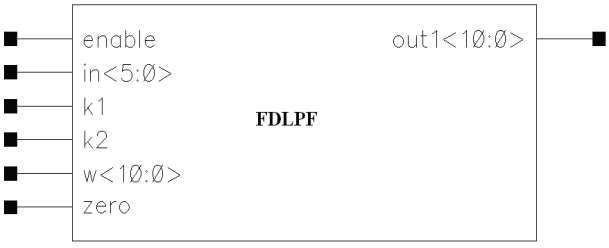

Figure 13. Symbol generation of FDLPF

D. Design of DCO

The DCO designed here consists of a delay cell and voltage controlled cell. Here designed block uses VHDL. The symbol generation of DCO using VHDL is shown in the Figure 14.

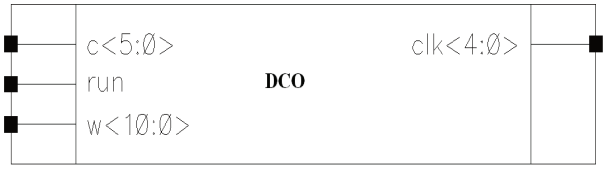

Figure 14. Symbol generation of DCO

IV. RESULTS

The entire designed ADPLL block uses are Cadence Virtuoso Schematic XL Editor and Cadence VHDL AMS Editor. The designed schematics use gpdk90nm technology. The spectre SPICE simulator using Cadence Analog Design Environment L-Editor is used for simulating the designed schematics. The Cadence Incisive Unified Simulator is used for simulating VHDL designs. The Cadence AMS Simulator is used for simulating entire ADPLL blocks. The simulation result of ADPLL shown in Figure 15.

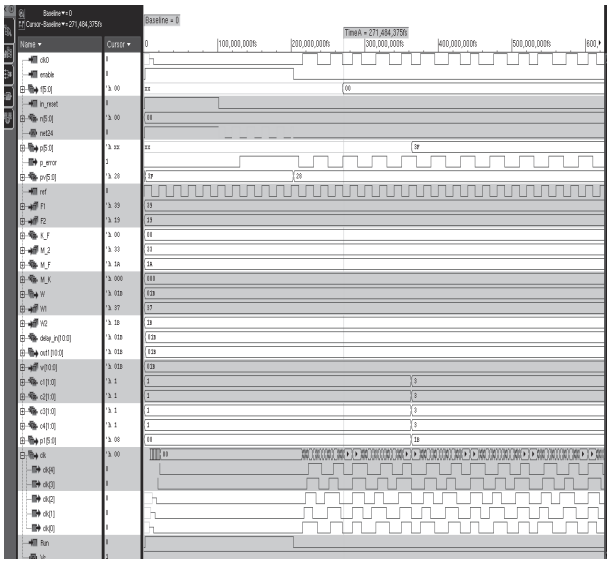

Figure 15. Simulation Result of ADPLL

Performance comparasions between existing and proposed ADPLL is shown in the Table I.

TABLE I

PERFORMANCE COMPARASIONS

Performance Parameter	Existing System	Proposed System
Process	0.18um	90nm
Power	11.394mw	962.75uw
Locking Time	3 cycles	2 cycles
Max.Frequency	416MHZ	625MHZ
Min.Frequency	4MHZ	10MHZ

V. CONCLUSIONS

In this paper proposed fast locking ADPLL uses VHDL-AMS. By using a feed forward compensation algorithm fast locking is achieved. The gpdk90nm technology is used to implement the design. The ADPLL frequency range is 10MHZ-625MHZ. The waveform results show that the ADPLL can complete frequency locking in 2 reference cycles, when locking to 271MHZ with 962.75uw power consumption. But in the existing system, the locking is achieved nearly after 3 cycles. So, the proposed ADPLL with feed forward compensation technique has more advantages than the existing methods. In LC block modifying with Digital Proportional integral controller (PI) locking time is reduced and used in low power application. Thus the fast and effective locking time is achieved based upon simulation.

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Efficient Place and Routing CAD Techniques for the Reduction of Power Dissipation in FPGAs

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Abstract: **The Computer Aided tools (CAD) are used to transform the design into a stream of '1's and '0's. This stream of bits is used to program the FPGA during the configuration time. Generally a huge number of programmable switches are used to implement FPGA. These switches are mainly used to implement functional blocks in FPGA. The CAD tools of FPGAs convert the design entered either using hardware description language or as schematic to a binary bit stream of '0's and '1's. During the configuration time, this bit stream effectively program the FPGA. On the CAD level, the packing and placement stages are modified to allow the possibility of dynamically turning OFF the idle parts of the FPGA to reduce the leakage power and as well as to reduce total power dissipation. A new activity generation algorithm is proposed and implemented that aims to identify the logic blocks in a design that exhibit similar idleness periods. Several criteria for the activity generation algorithm are used, including connectivity and logic function. Several versions of the activity generation algorithm are implemented to trade power savings with runtime. A newly developed placement and packing algorithm uses the resulting activities to minimize leakage power dissipation by packing the logic blocks with similar or close activities together. In this paper, the proposed architecture of FPGA using MTCMOS and the corresponding CAD tools save the average power of 30% in 90mm CMOS technology with less performance penalty.**

Key words—**Threshold voltage, CMOS, FPGA, CAD, Power dissipation.**

I. INTRODUCTION

Fueled by the increase in functionality and size of modern Field Programmable Gate Arrays (FPGAs), the market for FPGAs has witnessed a notable expansion in the past few years. This increase in demand has pushed FPGA vendors to design modern FPGAs using state-of-the-art CMOS technologies. Consequently, modern FPGAs suffer greatly from the deep submicron issues that affected the ASIC industry earlier along the technology scaling road. The biggest deep submicron challenge that hurdles further expansions of the use of FPGAs in the VLSI industry is leakage power dissipation. In order to face the ASIC industry the FPGA vendor must have less leakage power architectures and corresponding CAD techniques.

A. FPGA CLB Slice

The Configurable Logic Block (CLB) slice is the important logic resource of Xilinx Vertex-5 FPGA. It consists of 4 Look-Up Tables (LUT), multiplexers and carry logic. The complete Architecture of a slice in vertex-5 is shown in figure 1. In this slice 6-input logic functions can be realized by four 6-input LUTs and 8-inputs function also can be implemented with multiplexer by combining the outputs of two LUTs.

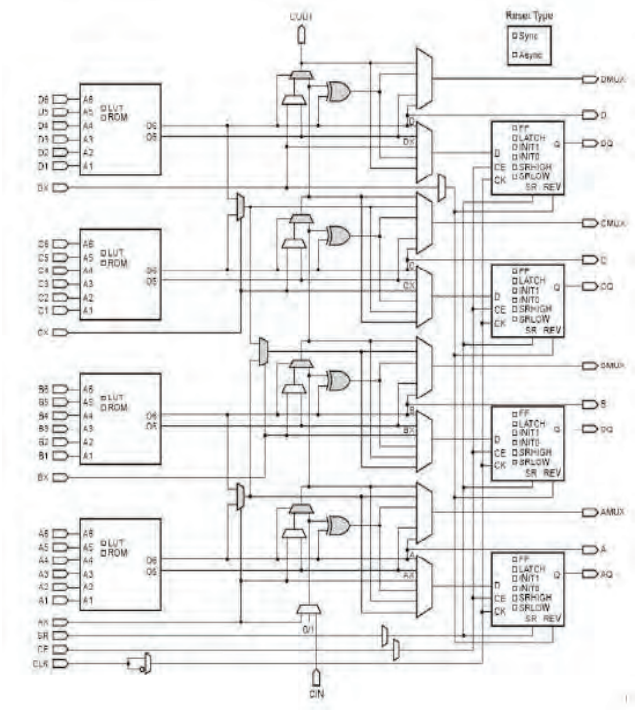


Figure 1: Xilinx's Vertex-5 slice architecture.

B. FPGA Routing Resources Architecture

The FPGA routing resources are divided into two categories which are segmented local routing and dedicated local routing. The connection between the logic blocks is done by using segmented local routing. The figure 2 shows the segmented local routing connections. These prefabricated wires in channels provide programmable connection between the logic blocks, switch blocks and connection blocks.

The dedicated routing is used to provide connection between global signals. Due to these global signals the logic blocks fan-out is increased. These are clock and reset, this gives low skew due to dedicated routing. These days some extra blocks PLLs and Delay Locked Loops (DLLs) are used in commercial FPGAs to further reduction of skew. In modern FPGAs, the different clock domains are available inside, to provide flexibility with respect to asynchronous designs.

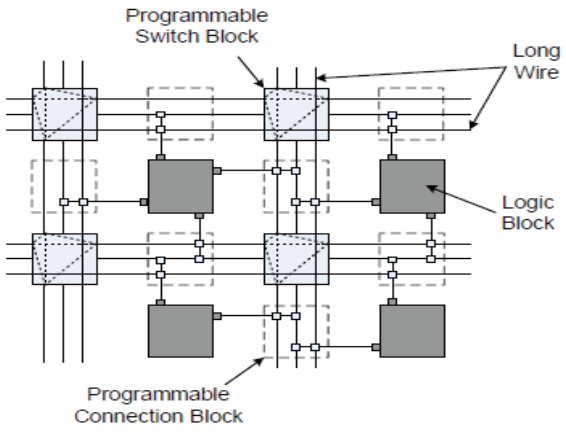


Figure 2: Routing resources in island-style FPGAs.

II. CAD FLOW FOR FPGAS

In an FPGA, to implement logic functions large numbers of programmable switches are required. For this programming, proper CAD tools are required. The CAD tools transform the design into the stream of bits, that program the FPGA during the configuration time. The design may be either entered as a schematic or Hardware Description Language (HDL). The CAD flow diagram of typical FPGA is shown in figure 3.

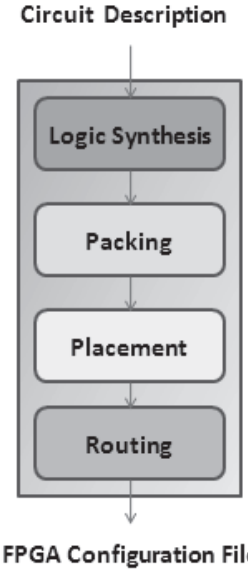


Figure 3: CAD flow diagram of typical FPGA

A. *Logic Synthesis*

Logic synthesis means the hardware description language is converted into equivalent net list of basic logic gates. The logic synthesis is performed in two stages which are "logic optimization" and "technology mapping" [2, 3]. The "logic optimization" is an independent stage that simplifies the logic function without using any technology information. At this stage logic redundancy is eliminated. In "technology mapping" stage, the optimized design is mapped into the corresponding Flip-Flops and LUTs in the CLB. Here each k-bounded logic functions are mapped with k-LUTs. This stage resolves the finding a set of k-feasible cuts. Hence the delay, power and area of the final implemented design are minimized. This technology mapping process is also called as covering problem.

B. *Packing*

The net-list of LUTs and flip-flops are converted to net-list of logic blocks using packing is shown in figure 4. The clusters of logic blocks from input net-list can be mapped into the physical logic blocks of FPGA. The packaging algorithms are used for minimizing the number of logic blocks, the delay along the critical path and the number of connections between the logic blocks. The physical limitations of the actual logic blocks of the FPGA have to consider the packing algorithms in view of total number of distinct input signals and maximum number of LUTs in a logic block.

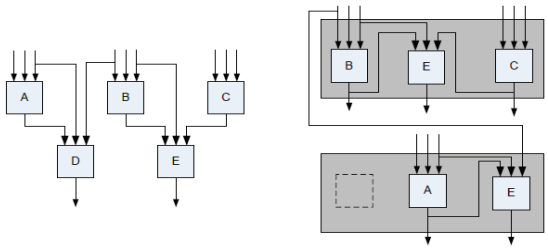


Figure 4: An example of packing.

The packing algorithms are categorized into bottom up [2, 4, 5] or bottom down [6, 7]. In the first algorithm, each cluster is formed individually around the main LUT until the cluster is full. Next, the second algorithm is concentrated on the partition of LUTs into clusters by using successive subdivision concept. The first algorithm is faster and simpler than second one because, only local connections are considered in the first method.

C. *Placement*

The packed logic blocks are distributed among the physical logic blocks in the FPGA by placement process. The delay along the critical path minimization and the resulting circuit routability is enhanced by the placement algorithms. There are three categories of placement algorithms; min-cut [8, 9], analytic [10, 11], and simulated annealing [12, 14] based algorithms. The Simulated Annealing (SA) placement tools depend on SA algorithms which are suitable for most of the commercial placement tools for FPGAs due to their flexibility to adapt to a wide variety of optimization goals [15]. First, for each logic block, the random initial placements are generated. Later, in order to improve the cost function a pair of logic blocks are selected for swapping as candidates at random. The candidate logic block is directly allowed if the cost function decreases, otherwise, the candidate logic block is allowed randomly, which decreases the process time of the algorithm. Finally, less number of swaps are placed in each and every iteration.

D. Timing Analysis

The placement and routing CAD tools in FPGAs are guided by time analysis [16] to obtain the speed of the routed and placed circuit and to identify the critical path during routing while estimating the slack of each source sink connection. A directed graph representing circuit is used for doing time analysis, where the nodes represent the LUTs or registers and the edges represent connections. The breadth first search method is used for finding the minimum required clock period for the primary inputs and to find the time arrival at node *i* is calculated from the below equation

$$T_{arrival}(i) = \max_{\forall j \in fanin(i)} \{T_{arriaval}(j) + del(j, i)\}$$

Here *del* (*j, i*) = delay on the edge between *j* and *i*.

Using the breadth search algorithm the required time at node *i* is obtained from the following relation starting from the primary outputs.

$$T_{required}(i) = \min_{\forall j \in fanout(i)} \{T_{required}(j) + del(ij)\}$$

Next, the slack on logic blocks connections between nodes *i* and *j* is obtained from the following equation

$$slack(i, j) = T_{required}(j) - T_{arrival}(i) - del(i, j)$$

The connections with zero slack in the logic blocks are called critical connections and connections with positive slack are called as non-critical connections, which are very long routed wires.

E. Routing

The different connections between the logic blocks in placed design of FPGA are programmed using routing resources or switches available, which is done in routing stage [13]. The main objective of the routing algorithm is to remove the congestion and delay in the routing resources and critical paths of FPGA respectively. In general, all the routing algorithms are classified into two groups which are detailed routers and global routers. Detailed routers assign the connections to specific wires in the FPGA, while global routers assign the connections by considering circuit architecture without looking at the number and type of wires available.

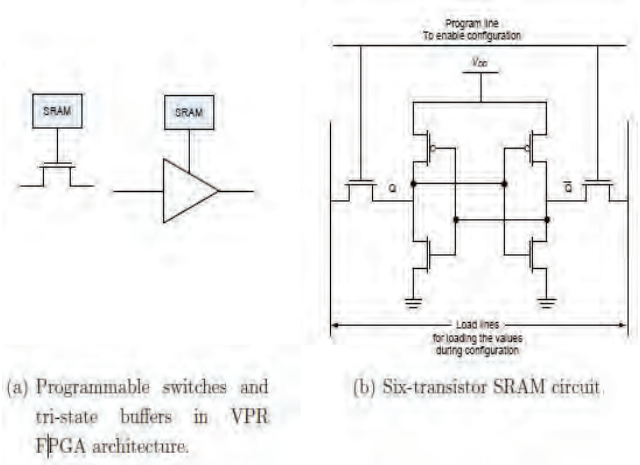
III. VERSATILE PLACE AND ROUTE (VPR) CAD TOOL

In this paper, the proposed CAD flow based on the Versatile Place and Route (VPR) is used for placement and routing in the FPGA. VPR is a popular placement and routing tool for FPGAs [13]. VPR is the core for Alter's modeling toolkit CAD tool [17] and it is preferred in a timing driven logic block packing algorithm in conjunction with T-VPack [4,12].

The VPR CAD tool contains two parts which are a placer and router. The optimum placement and route are found by interacting the placer and router components together for a given assets of conditions. This section gives the overview of VPR for FPGA architecture.

A. VPR Architectural Assumptions

The VPR architecture is assumed as SRAM based architecture and each SRAM contains configuration bits for all tri-state buffers and pass transistor multiplexers in the FPGA in both logic and routing resources shown in figure 5(a). The six transistor SRAM cells used in manufacturing SRAMs are shown in figure 5(b).



(a) Programmable switches and tri-state buffers in VPR FPGA architecture.

(b) Six-transistor SRAM circuit

Figure 5: The building blocks of SRAM programmable FPGAs used by VPR.

B. VPR Logic Architecture

VPR targets the hierarchal or cluster based logic architecture. In this architecture, a cluster of logic blocks are formed from the group of Basic Logic Elements (BLE). This each BLE consists of k- LUT and a 2:1 MUX and a D flip-flop as shown in the figure 6.

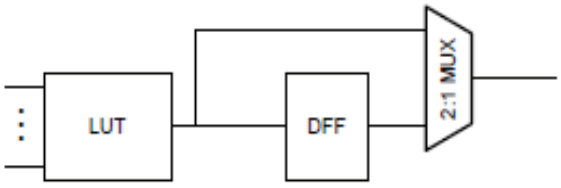


Figure 6: VPR BLE architecture.

BLEs inside the clusters are connected to each other. The input and output of the clusters are connected by using local routing which is shown in figure 7. The local routing is also used for connecting any of the inputs of BLEs to any of the outputs of the BLEs or any of the external inputs.

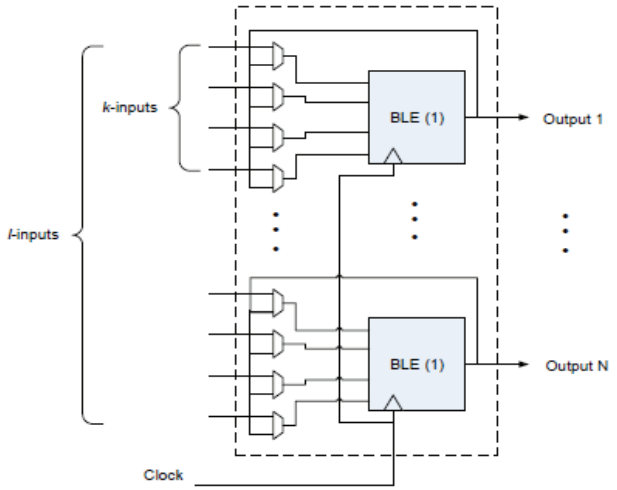


Figure 7: VPR logic cluster architecture.

The VPR logic cluster architecture consists of four main parameters in the FPGA architecture which are size of LUTs (k), no. of cluster BLEs (n), no. of external inputs of the cluster (I) and no. of external clock signals(Mclk). The LUTs in the VPR architecture are mainly implemented by small size transistors, then the parasitic capacitance of these small transistors are ignored.

C. VPR Routing Resources Architecture

In this section, the VPR routing resources architecture is presented. The VPR routing resources are characterized into 3 categories which are Switch block, Channel and wire parameters. The connections between input-output pads, channel width information is obtained by using channel routing resource. The channel width parameter includes the width of the vertical and horizontal routing channels, width of the input-output channel and no. of input-output pads of the one column or row of the logic clusters. The figure 8 shows the FPGA VPR architecture and routing model and the corresponding channel parameters.

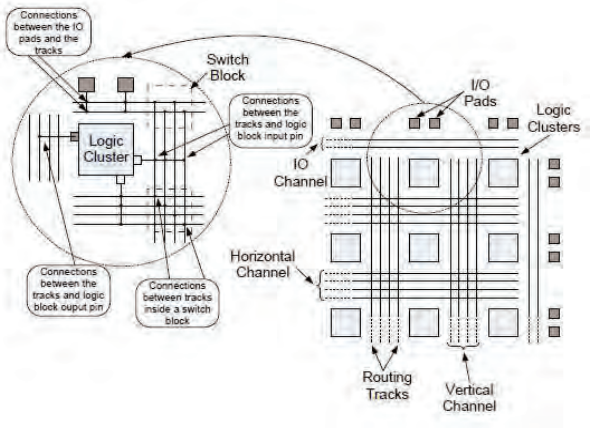


Figure 8: VPR FPGA routing architecture.

The switch blocks are used to make the programmable connection between the horizontal and vertical routing racks, and is shown in Fig. 8. The VPR characterizes the switch blocks by their resistance (R), input capacitance (Cin), output capacitance (Cout), connection flexibility (Fs), intrinsic delay (Tdel), switch type and switch block topology. The Fs - connection flexibility of a switch is defined as the no. of connections of the pins of the two sides of the switch. figure 9. shows the different topologies of switches supported by VPR.

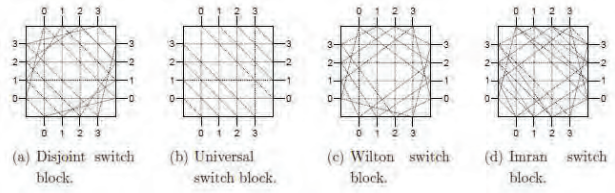


Figure 9: Switch topologies supported by VPR.

VPR describes wire segments by: the number of logic clusters spanned by the wire, the usage frequency of the segment in the FPGA, the resistance and capacitance per unit length, the switch type that connects the wire with other wires and the switch type that connects the wire and logic clusters.

D. Placement: VPR

The optimum algorithm for placement in VPR is basically an adaptive annealing scheme. This adaptive algorithm is called as Stimulated Annealing (SA), which is used to adapt the current placement at any instant of time. From the basic features of the circuit, the initial temperature is selected. Assuming that the total no. of functional block or logic clusters in the given design is denoted by n. The random initial placement is obtained, N cluster pair wise swaps are taken and initial temperature is evaluated as 20 times the standard deviation of the cost of the different n clusters. Moreover, the number of inner moves performed at each temperature is calculated as

$$MovesPerTe\ mparature = InnerNum \times N_{clusters}^{4/3}$$

Here innerNum is a constant and usually taken as 10. The way the temperature is updated is the feature of the adaptive SA algorithm used in VPR. Almost all moves are accepted at high temperatures and only improving moves are accepted at low temperatures in conventional Stimulated Annealing (SA). In adaptive Stimulated Annealing (SA) [13], the cooling technique tried to increase the time with respect to cost of the temperatures (low and medium temperatures) at the highly cost worsening temperatures using the following equation

$$T_{new} = \gamma \times T_{old}$$

Here γ is evaluated with respect to the % of moves accepted, as shown in table1.

Table 1: VPR temperature update schedule [13].

α	γ
$0.96 < \alpha$	0.5
$0.8 < \alpha \leq 0.96$	0.9
$0.15 < \alpha \leq 0.8$	0.95
$\alpha \leq 0.15$	0.8

E. Routing: VPR

The VPR CAD tool consists of two routing algorithms which are VPR routability driven router and timing driven router. The VPR routability is considered the path finding algorithm. The path finding algorithm repeatedly rips up and re routes all the nets of the circuit for every iteration. This process repeats until all congestions are completely eliminated. All available nets are initially routed to decrease the delay, but it produces congestion. Later routing iterations resolve the congestions by applying on overused routing blocks and resources. Then the cost is calculated for the given routing resource-n, which is connected to routing resource-m in the VPR and is given by

$$Cost(n) = h(n) \times b(n) \times p(n) + BendC(n, m)$$

Here h(n), b(n) and p(n) are historical congestion, base cost and present congestion respectively. h(n) is raised after every routing iteration in which n is overused. b(n) is set to the delay of n i.e. delay(n). p*(n)* is set to '1' if routing in which n is overused. p*(n)* is set to '0' if routing of n is not overused with congestion. The BendC (n, m) is used to detailed routability.

The timing driven router is based on path finding algorithm. In this case the timing information is considered for all routing iterations. The Elmore delay model equations are used to calculate timing information, delays and the cost of including a node n in a nets routing is given by

$$Cost(n) = Crit(i, j) \times del(n, topo \log y) + [1 - Crit(i, j)] \times h(n) \times b(n) \times p(n)$$

Here a connection criticality $Crit(i; j)$ is given by

$$Crit(i, j) = \max\left\{\left[MaxCrit - \frac{slack(i, j)}{D_{\max}}\right]^{\eta}, 0\right\}$$

Here MaxCrit is the parameter that controls how the connections slack impacts the congestion delay trade off in the cost function and Dmax is the critical path delay.

IV. CONCLUSIONS

This paper proposed several methodologies for leakage power reduction in modern nanometer FPGAs. The use of supply gating using Multi-Threshold CMOS (MTCMOS) techniques was proposed to enable turning OFF the unused resources of the FPGA, which are estimated to be close to 30% of the total FPGA area. Moreover, the utilized resources are allowed to enter a sleep mode dynamically during run-time depending on certain circuit conditions. To increase the benefits from the MTCMOS FPGA architecture, new packing techniques (AT-VPack, FAT-VPack, and T-MTCMOS) were proposed to include the logic blocks activities and pack those with similar activity profile together. The proposed techniques were applied to several FPGA benchmarks, and it was found out that the combination of R-LAP and T-MTCMOS for activity and packing algorithms respectively, yields the most leakage savings while incurring the minimum performance penalty. An average, the R-LAP and T-MTCMOS combination yields about 52% leakage savings, while the performance loss affecting the critical paths was kept at 3%.

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Implementation of Multi-Dimensional FFTs using FPGA

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Abstract—**This paper presents the implementation of multidimensional Fast Fourier Transform (FFT). In this implementation the FFT is calculated separately per each dimension in the pipeline. The resultant three dimensional pipeline FFT is implemented on an FPGA. The implemented FPGA can calculate the 3-dimensional (3D) FFT for a data which consists of 2563 samples with each sample with word size of 32- bits. The main challenge of this paper is the permutations between the one dimensional FFT modules. For these permutations, the storage memory is an external DDR2 SDRAM and on chip memory BRAM. The resultant multi-dimensional FFT is hardware efficient with very less latency around 84.2 msec.**

Index Terms—**DFT, FFT, FPGA, RAM, SDRAM & BRAM.**

I. INTRODUCTION

In the real world applications, the multi-dimensional FFTs are widely used. For example, the 2D FFT used in synthetic Aperture Radar [8], and 3D FFT used in astrophysics, motion detection cosmology, turbulence simulations[7], molecular dynamics and reverse tomography. At present, the iterative 2D and 3D FFTs are only implemented in the hardware, but the pipelined architectures are placed in 2D FFTs only. The aim of this paper is to design and implement a pipeline 3D FFT with stable throughput using external memory for permutations by supporting large number of input data sets. The motivation for this is to enable the use of 3D FFT in real-time systems demanding constant throughput of samples.

Generally, the discrete Fourier transform (DFT)is a different type of Fourier transform in the discrete manner set. The Cooley and Tukey invented the FFT in the year of 1965 [2]. The FFT algorithm reduces the total no. of calculations required to perform DFT. Since the FFT has been mostly used and is still used and research is being carried out today also. The entire FFT implementations are two groups of categories, one is iterative and the second is pipelined architectures. In the iterative architecture, one or more processing elements are reused for the calculation of the result. In the pipelined architecture, a series of processing elements are used to calculate result from sequence of samples. The iterative method is hardware efficient because it uses same hardware for many calculations but it is not suitable for continuous flow. For continuous flow environment, the less latency is required, which is provided by pipeline architecture with more hardware [3].

The same classification strategy is followed for the multi dimensional FFT(MD FFT) architectures. The MDFFT is also grouped into iterative and pipelined architectures. The iterative architectures which are discussed in[7,9] are designed as more flexible than the available processing elements. The performance of this is same as CDFFT only. The counter are pipelined architecture which supports the continuous flow of sample calculation by using dedicated hardware like 1DFFT.

II. ARCHITECTURE SELECTION

The architecture selection completely depends on the type of application in the real time environment. The tough constraints are considered for both latency and throughput. The typical example is a processing chain, in this each and every clock cycle provides data and gives the results in the same speed with required latency.

Another example in real time applications, is the post processing of the video stream is considered, in which the decision marker cannot take the correct decision in time if the latency is high. One more example is medical body scanning; for this application the doctor is needed to provide the information in time with respect to updates of the image, then low latency and higher throughputs are required.

A. Pipelined or Iterative Architecture

In real time applications there is requirement for fast computation of both 2D and 3D FFT. When we consider inside of the continuous flow, the iterative architectures halt a bit flow .The main reason for this is the memory loading and storing intermediate results by the repeated access.

For example, the 3D FFT have to read and write the data set 3 or 4times,than to process the chain and include a mandatory clock domain crossing (CDC) the bandwidth of memory also required 3 or 4 times. From the experience of CDCs, the debugging is tedious if the design is that in good manner. Hence, we can understand that the iterative process architectures are not fit for real time applications at the high cost of very advanced circuitry and large memories.

The pipelined architectures are basically adapted to a continuous flow of samples. This architecture enables the 1D FFTs to be evaluated without repeated memory accesses but hardware cost is high for mandatory permutations. The bandwidth of memory remains same for

the entire processing chain because memory uses only for read and write operations at once . For small data sets, the permutations with respect to on-chip memory only taken place with less hardware. The large data set permutations required external memory with some constraints and accessing limitations.

B. Memory permutations with some access limitations

In the implementation of 3- dimensional FFT, a two dimensional FFT is also considered as a part. Suppose if we are calculating the 2D FFT of each slice is spanned into two of 3 dimensions, followed by the calculation of 3D FFT. Therefore, the initial part of the 3 dimensional pipeline FFT is same as the pipelined 2D FFT as in the paper [3], namely a1D FFT followed by a transposition unit of the another 1D FFT. The transposition of permutations are present in both 2D and 3D FFTs. The 3 dimensional FFT performs another permutation between the 2nd and 3rd 1D FFT blocks, permutation has to permute the whole 3D dataset such that data is delivered in the 3 dimension to the 3rd1D FFT.

If the data is larger in size, one or both of those permutations have to perform in external memory. Hence, the large and high speed external SDRAM architecture is chosen to provide the required. The SDRAMs are dynamic in nature, so refreshing is required frequently, and you can access limited memory only at a time. This is the one difficulty while performing real time permutations for pipelined 3D and 2D FFTs. Basically, SDRAMs are burst oriented and at a time series of samples access is possible. That means the lowest address bits and corresponding elements are locked within the burst and permutated using separate auxiliary circuit. These permutations are not performed on SDRAM. In the auxiliary permutation circuit, the places of the bits are swapped and finally placed on their site.

Next, the memory SDRAM gets refreshed in a particular period of time without any loss of the data. This is considered as important constraint on the access of the memory schedule. The memory schedule can be done in two ways for refreshing, one is dynamic schedule and other one is static schedule. If dynamic schedule is selected, the latency is varied and sometimes throughput also varied, which is not supported by some applications. The other one is static schedule refreshing, in which refresh requires long time to fit with overhead by iterations with considerable bandwidth.

After that, for the rows and columns the less amount of memory access is only possible. Hence, the data is mapped to access the number of elements in all possible dimensions inside rows. For this sufficient row switches are required to overcome the overhead of the rows memory. The overhead concept is related to the process of pre-charging the active rows, the storing of the rows in the memory array, and fetching new rows and finally placing of those new rows in the sense amplifier blocks.

III. PROPOSED APPROACH

In this section, we focus on the 3D permutation between 2nd and 3rd 1D FFT. The series of 1D FFT architecture is selected with permutations in between; at the end we also perform a bit reversal result with natural order. The complete architectural view with bit reversal is shown in figure1.

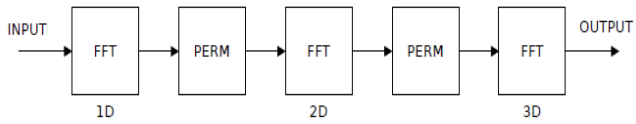

Figure 1. The complete view of the architecture for 3D FFT

The 3D permutation design process is also called as 3D rotation because this permutation rotates in three dimensions. This entire process is divided into following steps. 1) The determination of the external memory requirement, 2) identification of memory to fulfill the bandwidth requirements of the application and extraction of parameters to overcome the access 3) if external memory is not required, directly the design can perform permutations on internal memory i.e BRAM. 4) next step is determination of static schedule to avoid the tedious work to fulfill the latency and throughput always while using dynamic schedule, which includes group of memory commands for accessing.

In the design of the schedule, the row changes are not allowed during the schedule processing. If row changes are allowed, the data permutations inside the group is not performed without extra memory. Inside the group, the data index bits are locked when memory operations are performed, because the order is determined statically in the schedule. Due to this, finally the length of the schedule and size of the group are reduced and hence complexity and hardware usage reduced. The next step is, the permutation design and corresponding hardware to perform the permutation only. It means the number of locked bits impacts the 3D rotation. The placing of the bits should end up where the locked bits are located as low as possible, and preferably in the location to where we have to move the locked bits in the auxiliary permutation circuit after the memory. Otherwise, no auxiliary permutation is required for accessing the memory. Now, the counter bits are directly applied on memory according to the inverse permutation. We will need as many mappings as indicated by the *periodicity* of the required permutation. The last step is the auxiliary circuit design for permutation is based on the number of locked bits.

IV. IMPLEMENTATION

This section presents the implementation of the proposed 3D FFT, permutation circuits on FFT [4] and the transposition technique for FFT [3][10].The overall architecture of the system is shown in figure 2. This figure also shows the system modules and indexed bits and their order changing. In the any module the input and output

order is changed according to the order of the bits in the subs section of the module. By this, we can understand what is going on in the module. Based upon the inputs and outputs, all the modules are observed and duplicate things are ignored. The above process actually starts with the block FFT , then the process continues with the transposition and bit reversal in BRAM. This BRAM is followed by BDP circuits and it is continued with the 3D rotation in SDRAM. The auxiliary circuit for the required permutation circuit moves the locked index bits to finish the 3D rotation. The hardware usage and performance results are described below.

The 3D FFT with size of 2563 samples consists of indexed bits of 24 and 8- bits for dimension. This example is because it does not require 3d data set in cubic form and it is an easier case to understand the design. The above design is implemented on the DE3 board with the combination of a Stratix III FPGA including DDR2 of SDRAM slot. The goal of this paper is the designing of a system to give throughput of 200 M Samples per second and 1 sample per each clock cycle at the frequency of 200 Mhz.

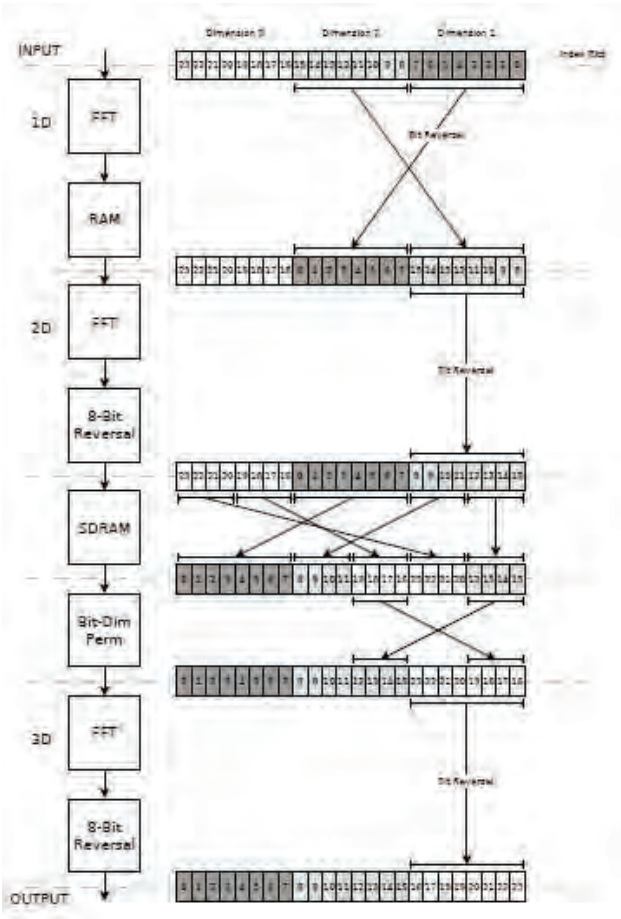

Figure 2.The system overview with bit positions of index at the input and output.

A. FFT

The placement of all identical FFT modules in the system are shown in the Figure 3.The 256-point feed-forward pipelined architecture considered. The multiplications approximation done by 14-bit precision CORDIC algorithm. From [1] the FFT module design is taken.

In the above figure, numbers specify the index bits and arrows gives the moment of the index bits done by the permutation. The shading portion in the above figure indicates the bit dimensions.

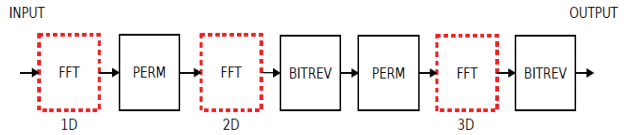

Figure 3. The FFT module highlighted system.

B. Transposition and Bit Reversal on BRAM

We need to perform two permutations between the first and second FFT Between the first and second FFT shown in figure 4. First permutation is bit reversal on the lowest eight bits for achieving natural order in the frequency domain, Second step is the transposition of matrix rows data in the second FFT. The next operation step is switching of index places for index bits on the one and two dimensions.

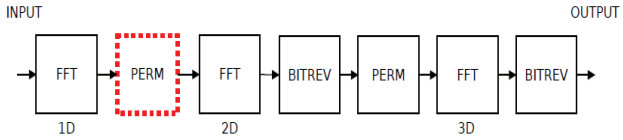

Figure 4. BRAM highlighted system overview.

For the saving of the resources, the two permutations are combined into one permutation performed on memory. This combining of permutations is easy because the BRAM did not have any access limitations and constraints. That means the read and write operations can take place any time. One and only limitation with respect to read and write operations is same location does not use double.

C. Bit Reversal

The following figure shows the bit dimensions and corresponding bit reversal circuits of the given design. This design performs the permutations using the minimum number of logic and memory resources with low complexity. This system is proposed in[4], which is desirable for efficient hardware design.

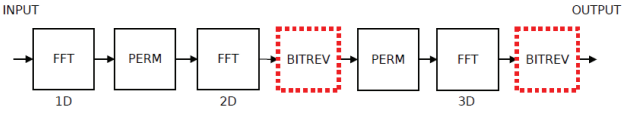

Figure 5. Architecture with bit reversal modules.

The bit reversal in FFT makes the samples in natural order with respect to frequency domain. After each FFT, the index bits reversed in the corresponding dimension is called bit reversal. In FFT architecture two bit reversal modules are included for permutations on memory. After the memory permutation for the first FFT, the transposition takes place. The auxiliary permutation circuit size is

increased in the SRRAM due to the placing of the bit reversal blocks for permutations in SDRAM. The size difference plays important role and bit reversal circuit sizes also. In the upcoming section, the sizes are compared with respect to SDRAM permutations.

D. Permutations on SDRAM

This section gives the design decisions and the corresponding implementations on the SDRAM memory. This is important criteria in the design. The following steps give the required permutations

Step 1 - Need of External Memory

Step 2 - External Memory Constraints and Parameters

Step 3 – Scheduling

Step 4 - SDRAM Permutation Design

Step 5 - Auxiliary Permutation Circuit.

Figure 6 and figure 7 shows the placing of the PERM block and the order of the input and output bits of the SDRAM respectively. Figure 8 presents the auxiliary circuit and corresponding input and output order with respect to permutations.

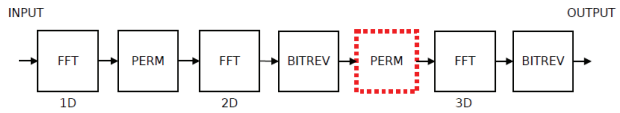

Figure 6. The SDRAM architecture and correction of the permutation blocks in the FFT system.

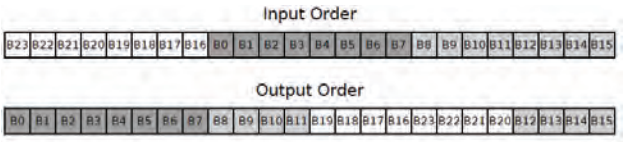

Figure 7. The input and output bit order in the SDRAM

The auxiliary permutation circuit permutes the last or lowest locked bits 19 to 16.

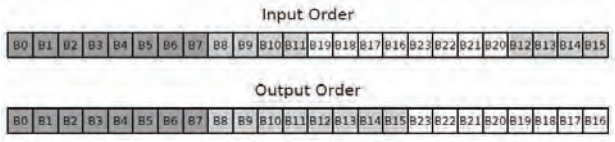

Figure 8. The input and output bit order of the auxiliary permutation circuit.

V. RESULTS

This section describes the key performance numbers in real-time systems, namely the latency and throughput. Latency, describes how long it will take for a value to propagate through the system. The throughput defines how many samples you can calculate per time unit; Based on this value you can then determine how many 3D FFTs you can calculate per time unit. The first 3D FFT calculation will be finished after the size of the data set divided by the throughput in addition to the latency. After that you will have one calculation finished after each following size of the data set divided by the throughput.

A. Throughput

In this system the system clock frequency is equal to throughput of the system. For the given system, the clock frequency is considered as 200MHz then the throughput is 200 mega samples per second. In this paper a 2563 cubic data samples are considered as example. The throughput for this example will be 11.9 frames per second, which is 84 milli seconds

B. Latency

The latency is determined with respect to number of implementation blocks in the system. The total latency is calculated using the propagation time of the samples with the aid of a counter. Final latency is determined using clock cycles. If the clock frequency is 200MHz then t_{lat} (latency) is given by

$t_{lat} = N \text{ cycles} * t_{clk} = 16848123.5 \text{ ns} = 0.084240615 \text{ s} = 84.2 \text{ msec}$.

C. Hardware Utilization

The size of the hardware depended on some factors. Mainly the design requires very high memory and logic registers of both the memories SDRAM and BRAM. The controlling of physical communication between memories, the corresponding delays and signals gives the utilization factor of SDROM. For this a Nios II soft processor is used as controller .This controller depends on utilization of on chip memory and utilization of logic. The on chip memory means the memory required for the matrix transposition. The remaining blocks are 3 FFT hardware blocks and permutation circuits. These permutation circuits consist of large number of memory elements, which occupies more logic registers since on logic blocks are used. Hence the calculation of FFTs is simple without any complex multiplications. The synthesis summary report and utilization of hardware presented in table I.

Table I. Synthesis results for hardware utilization on Altera Stratix III FPGA.

Family	Stratix III
Device	EP3SL150F1152C2
Logic utilization	28 %
Total block memory bits	2,548,445/5,630,976 (45%)
Memory ALUTs	2,595 / 56,800 (5 %)
Combinational ALUTs	19,955 / 113,600 (17 %)
Total registers	27048
Total pins	148 / 744 (20 %)
Total PLLs	1 / 8 (13 %)
DSP block 18-bit elements	0 / 384 (0 %)
Dedicated logic registers	26,870 / 113,600 (24 %)
Total DLLs	1 / 4 (25 %)

VI. CONCLUSIONS

This paper presented the 3D FFT algorithm design and implementation for continuously flow of samples using pipelined architecture. This paper is aimed for many real time applications. The FFT architecture is mainly based on series of three 1D FFT pipelined permutations. such a way that the data arrives in correct order to all three 1D FFTs, and that the result is in natural order in the frequency domain if this is desired.

This proposed and designed method can be used for any type memory system architectures, with or without access limitations and constraints. This implementation required two memories are on chip BRAM and external SDRAM.

This implementation is good competition for all the existing FFT designs in terms of cost , hardware, memory and performance. The further improvements in this design are including parallel dimensions in the permutations. Due to this modification, the fast memory using is possible by 1 D FFTs and then the throughput of the system is improved. It would be good to have the possibility to connect the design to a data bus and through it, a shared memory. The samples could be fetched from the data bus, and the shared memory could also be used for permutations. This would probably give a lower performance, but it would give a better opportunity to include the architecture in a complete System-on-Chip solution, and be more integrable in larger systems.

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DWT for Image and Video Compression using MATLAB

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Abstract— **Amount of data required to represent an image can be reduced by removing repetitive information which is known as compression of images. Today with the increase in the usage of computer, compression is very necessary. Because the space required for holding the uncompressed image outlays more. Fortunately, today image compression can be achieved by various methods. Although Video looks like ceaseless gesture, it is actually a series of halcyon images. The paper describes about the application of DWT methods for image and video compression. We also computed the PSNR and CR values after image reconstruction using IDWT algorithm.**

Index Terms—power, energy, Image compression, video compression, Discrete Wavelet Transform (DWT), Inverse Discrete Wavelet Transform (IDWT), Peak signal Noise Ratio (PSNR) and Compression Ratio (CR)..

I. INTRODUCTION

One image equals more than thousand words, unfortunately storing image outlays more than million words. Compression of image makes faster loading of web pages and it also saves a lot of bandwidth. Compression of image makes people to send photos easily which in turn reduces the bandwidth outlays and not make the recipient of the email angry. Therefore, compression is a necessary and essential for creating image files with feasible and transmittable sizes.

Video is a series of halcyon images which are called frames [5]. The consumer's use of the digital video increasing day by day, so video compression is necessary to curtail the size. There are two imperative benefits provided by video compression. First, it makes it potential to use the digital video transmission and storage environments that would not support uncompressed video. For example, modern Internet throughput rates are insufficient to handle uncompressed video in real time. Storage of uncompressed video on a DVD is possible only for a few seconds, so storage of video can be practical with video and audio compression. Secondly efficient usage of transmission and resources can be achieved by compression of video. If a high bit tare transmission channel is available, then it is a more alluring proportion to send a high resolution If a high bit rate transmission channel is available, then it is a more alluring proposition to send a high resolution compressed v ideo or multiple compressed video channels than send a single, low resolution, uncompressed stream. Even with consistent advances in the stockpile and communication capacity, the essential component of multimedia services for many years to come is compression. In a listless compression system analytical repetition is removed so that the authentic signal can be perfectly reconstructed at the receiver. Unfortunately, at the present time lossless methods can achieve only small amount of compression of image and video signals. Most practical video compression techniques are based on the lossy compression, in which preeminent compression is achieved, but decoded signal not identical to the authentic. A video compression algorithm is used for adequate compression with less low.

II. ONE-DIMENSIONAL DWT AND IDWT ARCHITECTURE

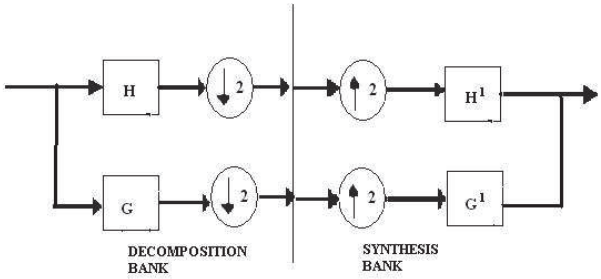


Figure1. One Dimensional DWT and IDWT

The universal form of 1 D DWT is shown in above figure [3]. Here the discrete signal is passed through a low pass and high pass filters H and G then down sampled by factor 2 completes forward wavelet transform. The inverse is obtained by up sampling by a factor of 2 and then using the reconstruction filters H1 and G1. The low pass (H) and high pass filter (G) combined called as decomposition (analyze) filter bank [6]. The low pass (H1) and high pass (G1) filters are combined called as the Synthesis filter bank [6]. Analyze filter banks are used for compression and synthesis filter bank is used for decompression

III. TWO-DIMENSIONAL DWT AND IDWT ARCHITECTURE

Image is two dimensional signal which is denoted by X (m, n) here m is the number of rows and n is the number of columns. So for image compression, first we apply DWT Algorithm to rows followed by columns. We can interchange the order of rows and columns means we first apply DWT algorithms to the column first followed by rows next. Similarly, IDWT algorithm also applied to the

columns followed by rows completes the reconstruction of images. The following figure shows the level one DWT and IDWT architecture for images [3], [4].

Figure2. Level One DWT for images

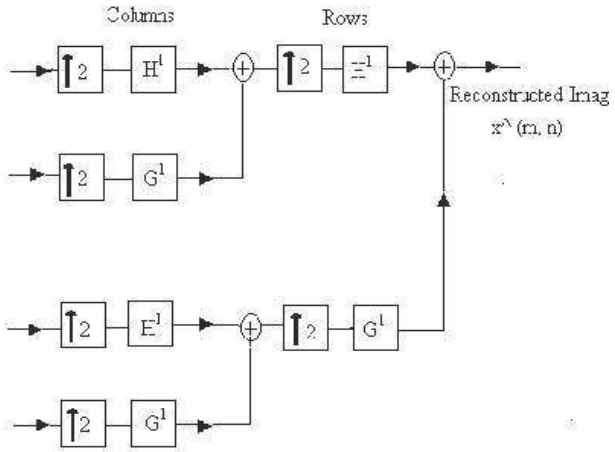


Figure3. Level One IDWT for images

High pass filter output values are called as "detail coefficients" [3] and the output values of low pass filter called as approximate coefficients [3]. Detail coefficient values are less significant in image reconstruction even though we neglect these values we get back the original image with less loss.

DWT FOR 2 D IMAGES

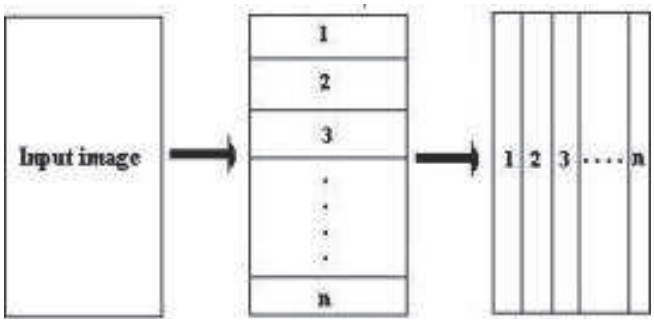


Figure4. Applying DWT to images for compression

Wavelet transformation entails transformation of image data horizontally first and then vertically. Here the image plane is divided into n horizontal sections which are horizontally transformed concurrently. After then the image is divided into n vertical sections which are then vertically transformed concurrently. It is not a must that the number of horizontal sections is equal to the number of vertical sections.

IV. CR AND PSNR

A touchstone in compression of image data is the compression ratio and PSNR (Peak Signal to Noise Ratio) [5]. The compression ratio is used to measure the amount of data compressed by comparing the size of the compressed image and original image. The preeminent the compression ratio means the better the wavelet functions. PSNR is another important parameter used to calibrate the image nature [8]. PSNR parameter is always used as a touchstone to find the closeness between reconstructed and the original image. Better image quality can be achieved by larger PSNR value [1].

$$\text{Compression Ratio} = \frac{\text{The size of compressed Image}}{\text{The size of the Original Image}} \text{ ------ (1)}$$

PSNR defined as follows [2], [3]

$$PSNR = 10.\log \left| \frac{255}{\sqrt{MSE}} \right| \text{ ---------- (2)}$$

Where MSE is mean square error,

$$MSE = \sum_{m=1}^{M} \sum_{n=1}^{N} (X(m,n) - X^{\wedge}(m,n)))^2 \text{ ------(3)}$$

V. IMAGE COMPRESSION RESULTS

A) Level – One Compression results

Figure5 (a) baboon image

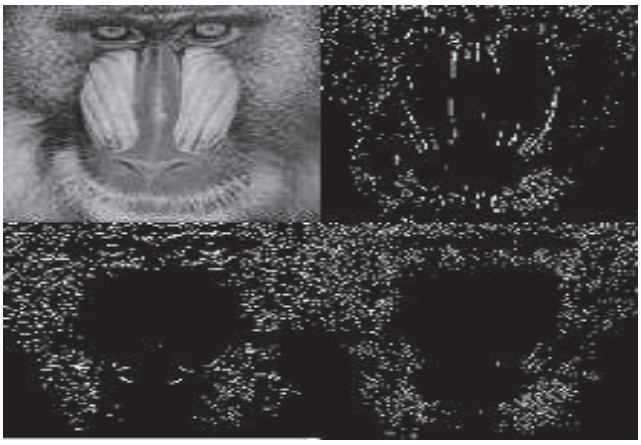


Figure4 (b) Level one DWT

Figure5 (b) Level one DWT
(Detail coefficient values enhanced by thresholding)

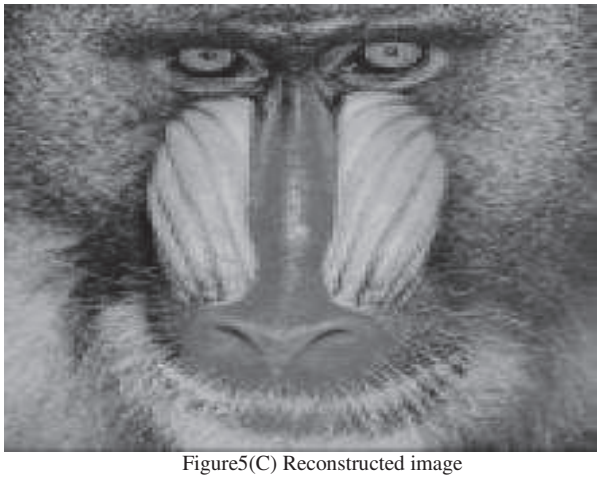


Figure5(C) Reconstructed image
(Only Approximate coefficient values are used)

Figure5 (d) Difference between original and reconstructed
(Coefficient values enhanced by thresholding)

Here we got the compression Ratio of '4' and PSNR 34.1dB. Here the detail coefficients values are enhanced for better view. Thresholding mechanism it used to enhance the values. Here threshold value is 20, means all the above 20 are forced to 255 and below 20 are forced to zero.

B) Level – Two Compression Results

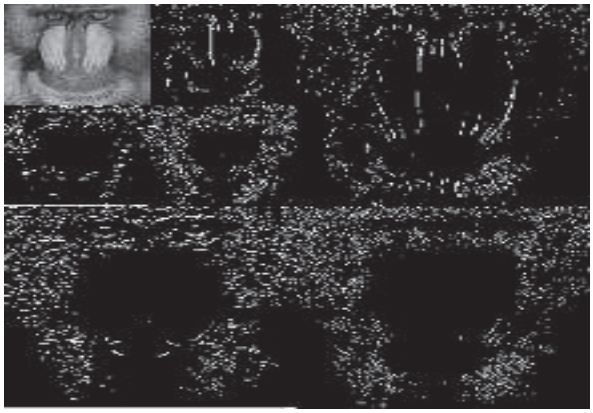


Figure6 (a) Level Two DWT image

(Detail coefficient values enhanced by thresholding)

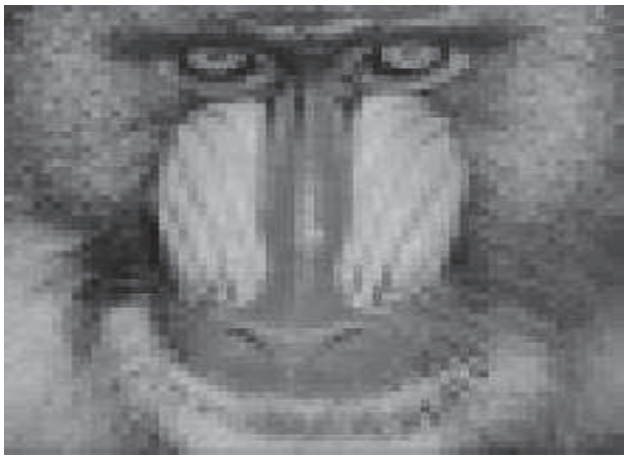


Figure6 (b) Reconstructed images

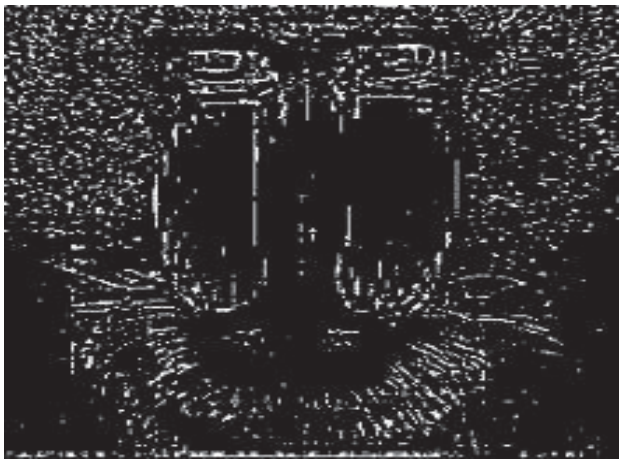


Figure6 (C) Difference between original and reconstructed
(Coefficient values enhanced by thresholding)

Here we got the compression Ratio of '16' and PSNR of 32.44 dB. Here the detail coefficients values are enhanced for better view with the threshold value of 20.The difference between authentic and reconstructed image figure (5(c)) increased in level two DWT results compared to level one DWT results (figure(5(d)). Observe that the PSNR value is decreased in level two DWT means the reconstructed image quality is less. As compression Ratio increases, the reconstructed image quality decreases.

VI. VIDEO COMPRESSION RESULTS

A) Level - one Video Compression Results

Although video look like ceaseless gesture, it is actually a series of halcyon images, and changing fast enough that it look like ceaseless motion, so video compression is similar to image compression .Video compression is done when we compress all the frames in that video. Here I have taken VIP TRAFFIC video which consists of 120 frames in it. Here some of frames results are shown.

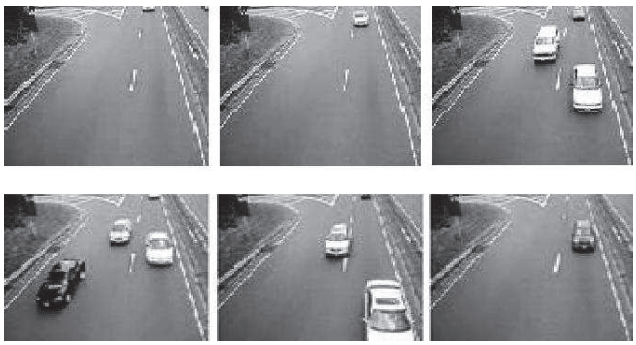


Figure6 (a) some frames in Video Traffic

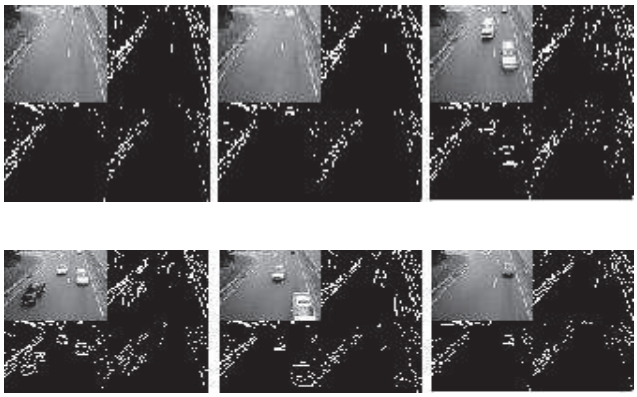


Figure6 (b).Level one DWT for frames
(Detail coefficient values enhanced by thresholding)

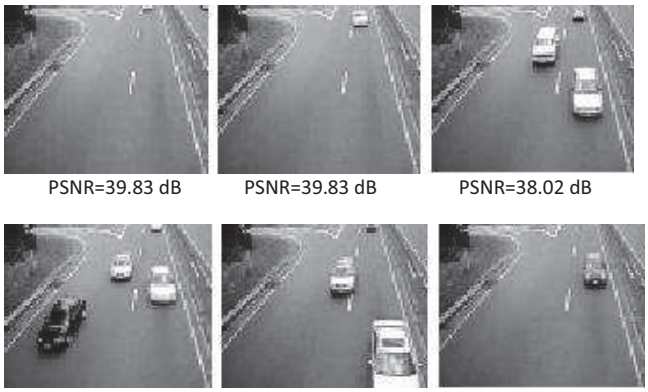
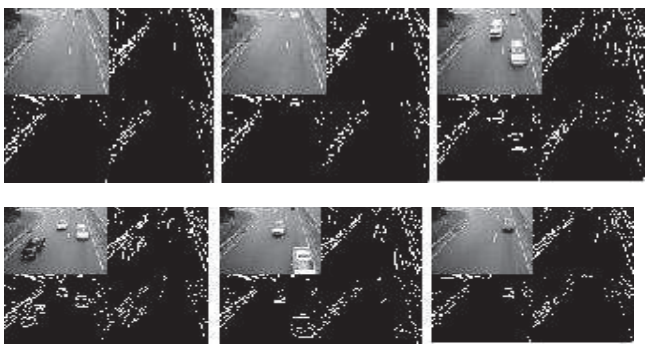


Figure6 (c). Reconstructed frames with PSNR values
(Only approximate coefficients are used)

B) Level – Two Video Compression Results



7 (a).Level –Two DWT for video frames

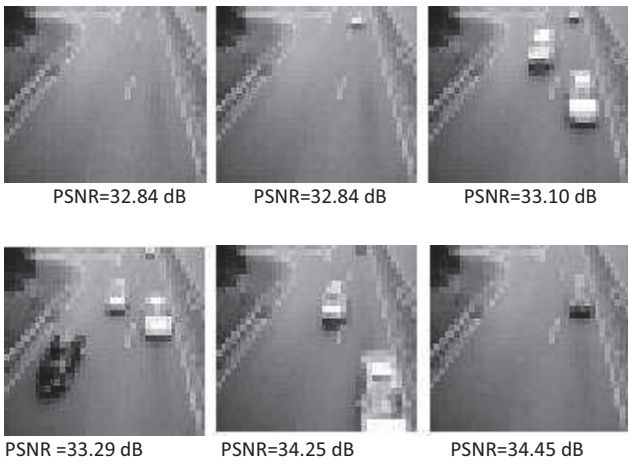


Figure7 (b). Reconstructed frames with PSNR values
(Only approximation coefficients are used)

Compression Ratio (CR) is 4 for one level compression and 16 for two level compressions. PSNR value decreasing in level two compressions compared to level one compression, it means the reconstructed image quality decreasing and error between original and reconstructed image is increasing. Larger PSNR will produce better image quality

TABLE 1
Results of video Frames

Compression Ratio	PSNR(DB)	Level Of DWT
4	39.83	1
16	33.83	2

VII. CONCLUSIONS

Digital video compression techniques have played an important role in the world of telecommunication and multimedia systems where bandwidth is still a valuable commodity. Hence, video compression techniques are of prime importance of reducing the amount of information needed for picture sequence without losing much of its quality, judged by human viewers. Here we have used Discrete Wavelet Transform (DWT) to achieve the compression for the image and it is extended to a series of images which is nothing but a video. PSNR and Compression Ratio are calculated in this paper. PSNR value is decreasing as the compression ratio is increasing, this means that the reconstructed image quality is decreasing.

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Implementation of Memory Controller using Cadence Tools

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***Abstract*—The Controller is designed which allows a high degree of programmability and interfaces many other memory devices which will be very flexible in nature to be programmed with other devices. To achieve throughput or latency multiple abstraction layers are present. The Controller provides the access of memory, executes in parallel form which leads to less logic utilization. This type of memory controllers are used in double data rate synchronous dynamic random access memory. The Memory Controller and Core Memory Controller are implemented using Cadence ASIC 45nm technology. Blocks are tested using ncvlog simulator, RTL schematics are generated using RTL Compiler and finally GDS-II file is obtained by using SoC Encounter. So the proposed Double data rate synchronous dynamic random access memory controller works with very less logic utilization, route and offset delay.**

***Index Terms*— Memory Controller, Core Memory Controller, Arbiter, ASIC Cadence- RTL Compiler, and SoC Encounter.**

I. INTRODUCTION

As with standard Synchronous dynamic random access memory [6] the design is pipelined and consists of various register banks which allows parallel operation to achieve higher bandwidth [1]. It performs read, write instructions by varying the length size i.e., 2, 4 or 8. A double data rate Synchronous Dynamic Random Access Memory consists of four register banks where as each register bank consists of multiple rows. Further, each row is divided into columns and consists of 32 bits of data. The number of rows and columns are reliant on the size of the on chip memory. The memory organization with four register banks will be executed with single command operation. Due to the size of the data bus, we cannot perform more than one write or read instruction. When one row is performing either read or writes operation, the other rows can be pre charge and activated to access the register bank. The schematic view of double data rate SDRAM is shown in the figure 1.

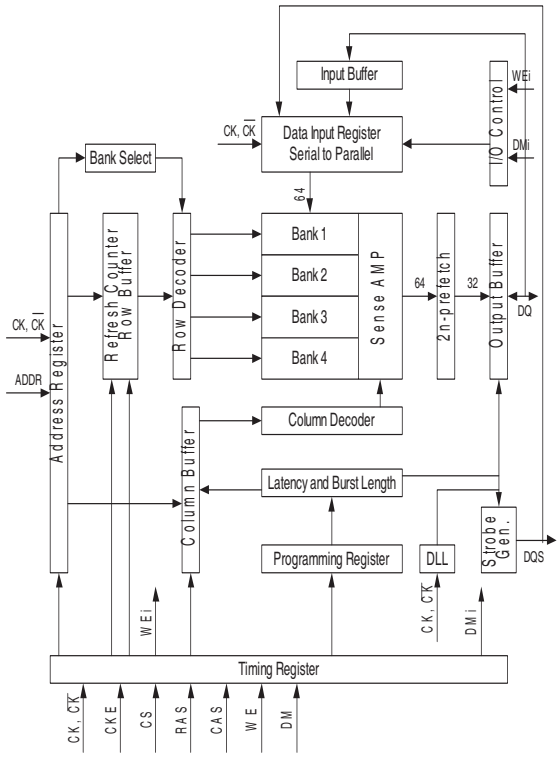

Fig 1: Schematic View of Double data rate

II. BLOCKS EXPLANATION

A. *EXTENDED REGISTER SET*

The Register set [4] and extended register set control word formats are used for writing data, which defines the specific mode of operation. The extended register set is shown in the below figure 2.

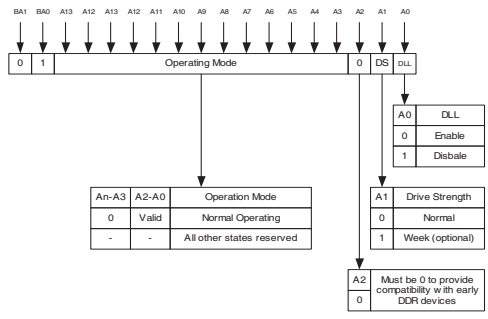

Fig 2: Extended Register Set

B. AHB INTERFACE

The Advanced High performance Bus Interface is a receiver interface as shown in figure3. The bus [3] acts as an input for the accessing port to the on chip memory and even for all the intellectual property cores which are present on the controller. The advanced high performance interface informs to the core memory controller about the starting location of the data when a read operation approaches the bus. The data is buffered and as soon as the interface has started to receive data from the DDR SDRAM it presents the data on the AHB bus. As soon as the write operation approaches the interface will store the data into the memory controller. Compared to random access memory, the advanced high performance bus works on lower frequencies for that purpose when the data appears the data will be registered before the write instruction is started.

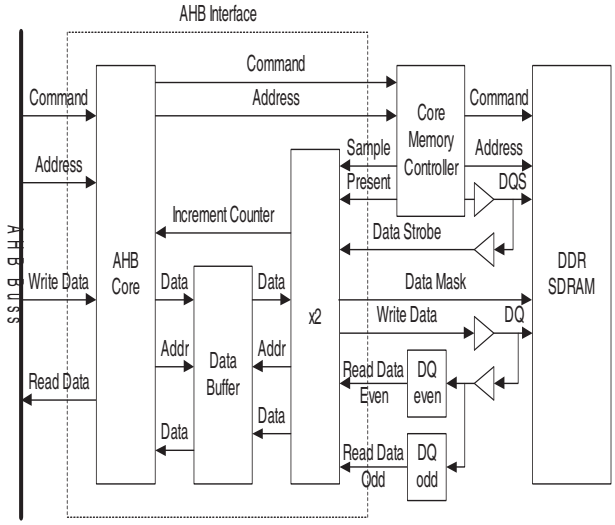

Fig 3: Schematic View of AHB Interface

C. MEMORY CONTROLLER

The Memory Controller [2] as shown in figure 4 is implemented to support a multiple advanced high performance bus receiver interfaces. For this purpose the two paths have been separated i.e., control path and data path. The core memory controller handles the control path and the data path which are inbuilt in each of the AHB interface of the core memory controller. The access of the data path, control path will be decided by the internal arbitrator. Advanced Peripheral Bus is used for the purpose of initialization. The memory controller is supported to handle multiple random access memory chips and other memory devices for the synthesis.

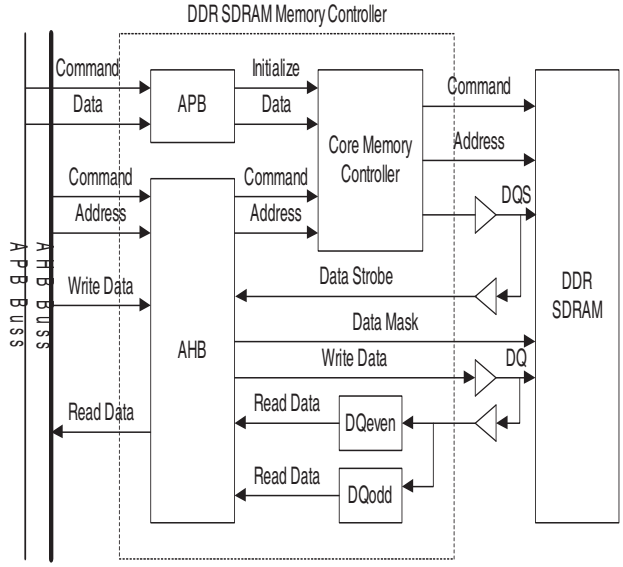

Fig 4: Schematic view of Memory Controller with AHB interface

D. CORE MEMORY CONTROLLER

The main purpose for the implementation of on chip core memory controller is to control all the command of instructions in multiple timings and all the activated rows will be present in the form queue. The main feature of arbitrator is that it will inform the current operation process and the next operation which is going to be executed because the activation of the rows will take huge amount of time. This function can be possible to activate the row ahead when the next instruction is not using the same register bank as present instruction. The on chip core memory controller divides the burst into multiple instructions which are useful to perform the entire burst operation as shown in the figure 5. The core memory controller also handles the activation of the next rows which are going to be executed.

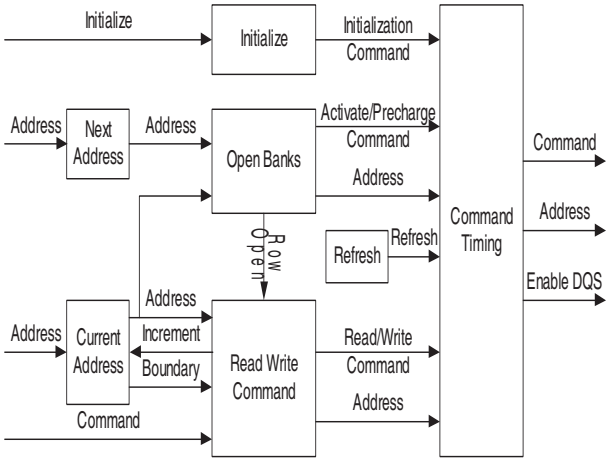

Fig 5: Schematic View of Core Memory Controller

E. ARBITER

As shown in figure 6 it is more advantageous to have multiple advanced high performance bus interfaces compared to having single bus interface [3], by adding more bus interfaces it leads to increase the transfer data rate of the device. The arbitrator is implemented by using round robin protocol or round robin with priority. The arbitrator will decide how many bus interfaces are required to implement the memory controller. By using the implementation of arbitrator with round robin fashion, it supports two advanced high performance bus interfaces. This makes the construction of arbitrator very simple because any additional functionality block is not necessary to decide which device of advanced high performance bus interface should grant the access for the current instruction if any instructions are in the form of queue.

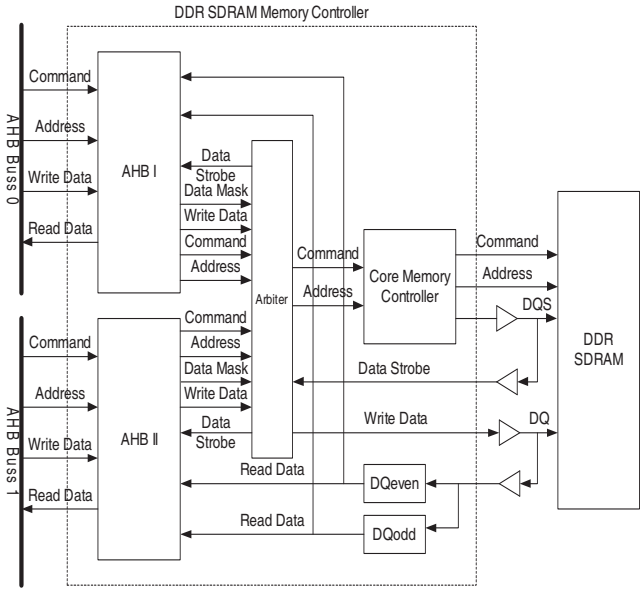

Fig 6: Schematic View of Memory Controller with 2 AHB Devices

III. BACKEND PROCESS

A. PLACEMENT

The placing and routing were performed by using SoC Encounter tools [5] for the 45nm technology TSMC libraries to obtain the layout structure for the device and it takes 70% of core utilization. The pads (GND, VDD) will be surrounded by the core in all the four directions (top, bottom, left, right) with subsequent width and length. The placement of memory controller is shown as is figure 7.

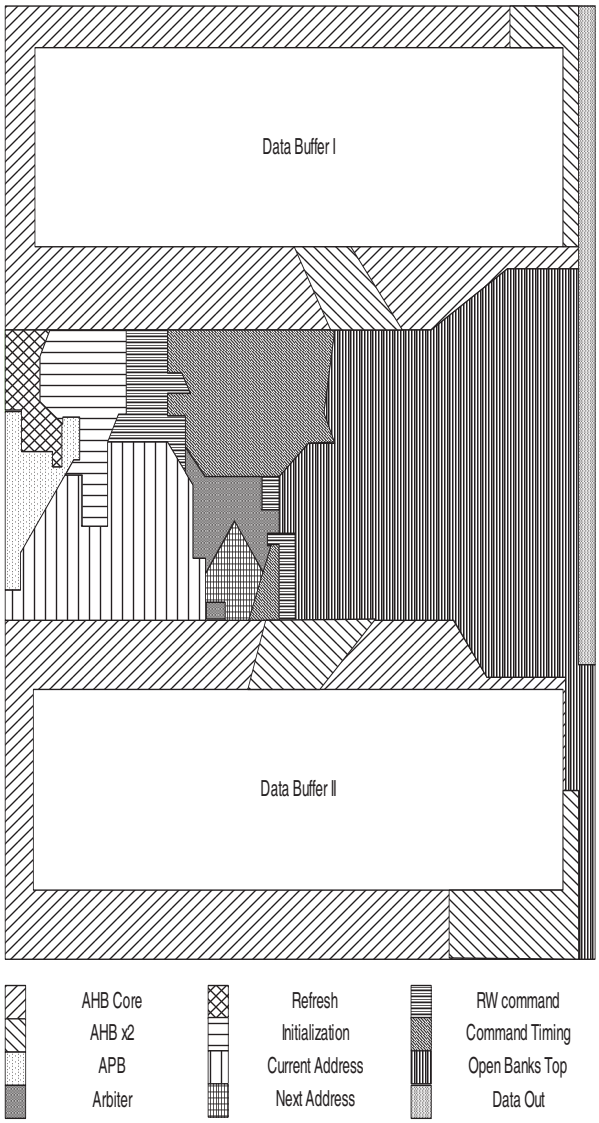

Fig 7: Placement

IV. IMPLEMENTATION RESULTS

All the blocks are implemented by using ASIC Cadence SoC Encounter tool with 45 nm technology libraries. Figure 8 shows RTL Schematic of Memory Controller, Figure 9 shows RTL Schematic of Core Memory Controller, Table 1 gives the pre, post clock tree synthesis report when it performs routing and finally figure 10 shows the IC chip fabrication layout structure which is named as GDS II file.

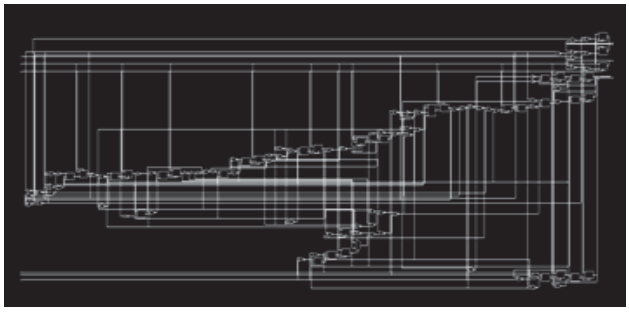

Fig 8: RTL Schematic of Memory Controller

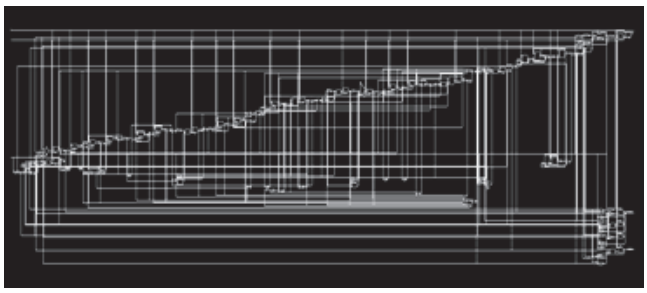

Fig 9: RTL Schematic of Core Memory Controller

Setup Mode	Pre CTS Report Analysis	Post CTS Report Analysis
WNS (ns)	2.807	2.790
TNS (ns)	0	0
Violating Paths	0	0
All Paths	122	122

Table 1: Pre and Post CTS Report Analysis Report

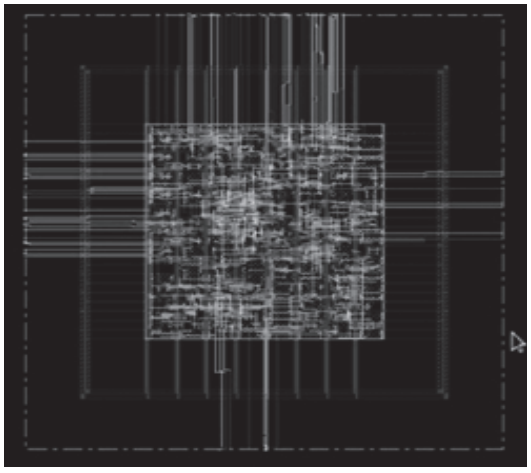

Fig 10 : GDS II File Core Memory Controller

V. CONCLUSIONS

All the blocks are verified by Ncvlog simulator and synthesized by using RTL Compiler and finally implemented on SOC Encounter and obtained IC chip layout i.e., GDS II file. The main advantage of memory controller is high through put or high latency. This type of memory controllers are used in random access memory devices. It provides layers of abstraction to achieve maximum throughput. It can be applied in personal computers and storage devices. As future work in place of two AHB bus interfaces more number of devices can be implemented to improve the performance of controller.

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A Low Power, Leakage Reduction, High Speed 8-Bit Ripple Carry TSPC Adder using MTCMOS Dynamic Logic

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Abstract- **In Every IC design adder is basic building block to perform arithmetic operations. This paper presents new TSPC (True Single Phase Clock) adder for 8-bit operations using MTCMOS dynamic logic. The proposed design comprises of 18-transistors instead of 21-transistors used in existing design. The design also has advantage of power trade-off where it consumes only 384.5pW with reduced leakage power from 96 to 99% in sleep mode of circuit operation. MTCMOS Dynamic technology includes both HVT(High V_{TH}) and LVT(Low V_{TH}) Cells. HVT Cells are used as power switch and LVT Cells are used for actual logic operation to increase speed performance of the circuit. Conventional CMOS logic has more static power dissipation. In this paper MTCMOS dynamic logic is introduced to eliminate static power dissipation. The proposed design is implemented using 45 nm technology with supply voltage(V_{DD}) of 1V.**

Index Terms-**TSPC, CMOS, MTCMOS, Power, Sleep mode**

I. INTRODUCTION

Adder is a very essential component in digital computing systems such as DSP processors ,FPGAs, Floating-point processors. In Microprocessors, adder has special role as it is used for address generation for data access as well as it used as functional blocks to design Multipliers. In recent trends VLSI design technology has scaled down from micron, deep sub-micron to nanometer technology [1]. Power supply is an important factor of interest in research area where the scaling down key lies based on minimizing the threshold voltage of MOS-transistor. CMOS technology[2] is being used for less power dissipation,but, it has a limitation of static power dissipation and more leakage power due to single threshold voltage (V_{TH}) transistors. There are many technologies that have more than one threshold voltages(V_{TH}), like dual-VTCMOS, MTCMOS, VTCMOS and etc. Among which MTCMOS logic is most useful approach for less power consumption and less leakage power.

The TSPC (True Single Phase Clock) adder has only single phase clock for easy clock distribution throughout the logic and avoids clock skew problem effectively. The circuit will be evaluated when clock signal is high and tristated when clock signal is low. This paper presents simulation results for single bit full adder as shown in section IV and the proposed design has conclusion in section V.

II. MTCMOS DYNAMIC LOGIC

Multi threshold voltage CMOS (MTCMOS)[3] logic is to improve speed performance and less power consumption. Leakage reduction is also very important key parameter by using MTCMOS logic. With the help of this technology the portable systems like Laptop, Mobile phones etc have more battery life and backup time.

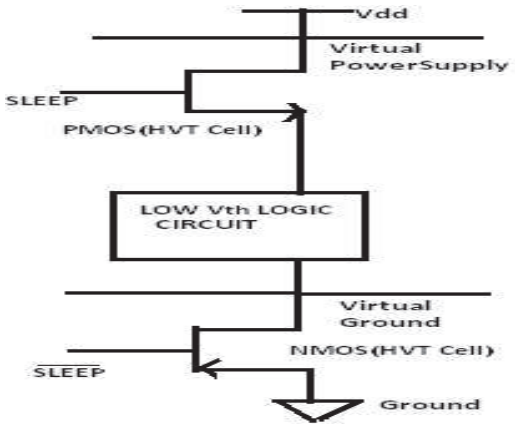

Fig 2.1 General MTCMOS Dynamic logic

In general a transistor has less threshold voltage (V_{TH}) will switch faster, a transistor has more threshold voltage(V_{TH}) will reduce static power dissipation.

The MTCMOS logic is composed of both transistors which have low threshold voltage(LVT cell) and high threshold voltage(HVT Cell). Fig 2.1 shows basic MTCMOS Logic in which HVT cells are used as power supply switches and LVT cells are used as actual logic operation to better speed performance. MTCMOS logic will work in two modes one being *active mode* in which

HVT cells (Sleep transistors) are switched to ON for logic evaluation. Second mode is *standby mode (idle mode) where* HVT cells (Sleep transistor) are switched to OFF state for reducing leakage power.

In general, MTCMOS logic has high V_{TH} PMOS transistors connected between Power supply (V_{DD}) and low V_{TH} logic,and high V_{TH} NMOS transistor is connected between low V_{TH} logic and ground. In this paper only high V_{TH} NMOS transistor is used as shown in Fig 2.2 for better performance and avoids bounce noise at ground.

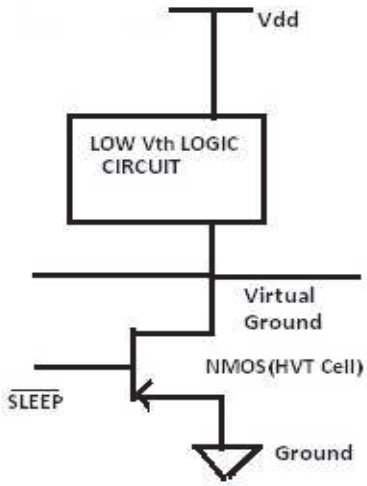

Fig 2.2 Single Sleep transistor MTCMOS Dynamic logic

III. PROPOSED SYSTEM

The proposed design has 18-transistors for one bit TSPC full adder shown in Fig 3.1.The existing design has 21 transistor with low performance [4], this design has decreased silicon area from 15 to 20 % with high speed performance and less power consumption. It has dynamic operation with the help of single clock signal. The output will be considered when the clock signal is high, and output is floated when the clock signal is low.

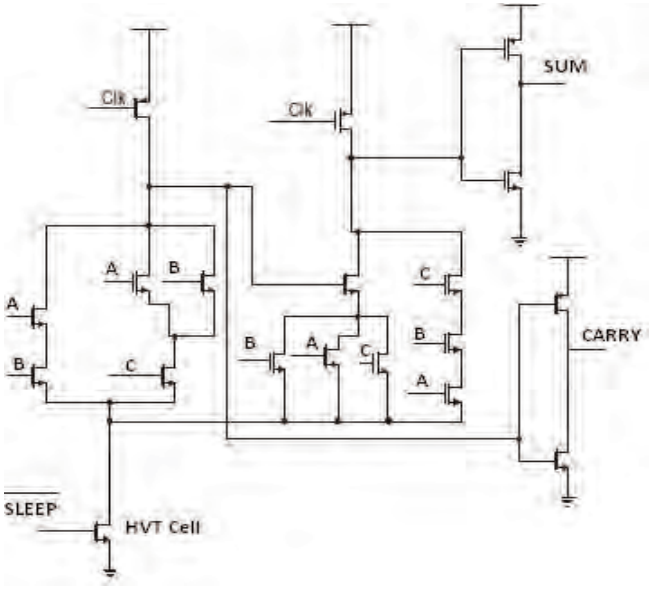

Fig 3.1 A Single bit TSPC adder with 18 transistors (Proposed)

The design logic built with low threshold voltage transistors (LVT) which has faster switching with no penalty of power consumption, and additional HVT cell is used for power switch i.e, if circuit is in idle mode the power switch will be OFF to save the power and to reduce the noise. The basic full adder logic has three inputs and two outputs shown in Fig 3.2

Sum =a xor b xor c

Carry =ab+bc+ca

Fig 3.2 One bit Full Adder block diagram

Ripple Carry Adder: Eight-bit ripple carry adder [5] is group of eight 1 bit full adders in which carry output of one full adder is one of the input for next full adder as shown in Fig 3.4. The design can be further used in hierarchical form to implement 16-bit, 32-bit adders. The 1-bit full adders are arranged in a manner from left to right where S_0 is LSB bit and S_7 is MSB bit. The carry is propagated through each adder, where the first full adder carry input is assumed as logic '0'.

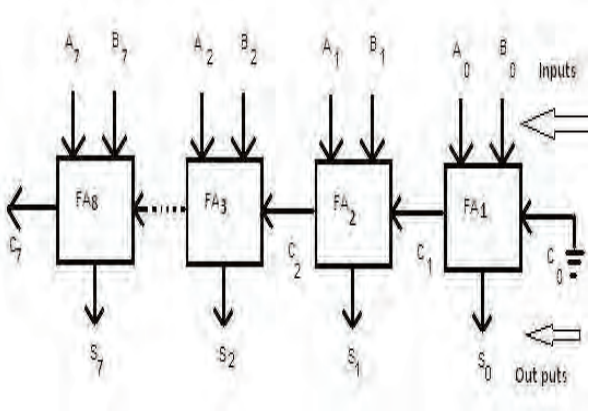

Fig 3.3 8 bit Ripple carry Adder block

IV. RESULTS

The 8-bit Ripple carry TSPC adder is designed and simulated using Cadence Virtuoso Schematic editor XL in 45 nanometer technology with supply voltage of 1V. The 1-bit TSPC full adder schematic diagram shown in Fig 4.1 is simulated using Cadence Analog Design Environment (ADE_L) [6].

A 4-bit adder is constructed from the four 1-bit full adders, and further a 8-bit full adder is constructed from two 4-bit full adders. First 1-bit full adder is simulated for different input combinations is shown in Fig 4.2. Consequently, design is verified for 4-bit, 8-bit full adders. The 8-bit adder block diagram is shown in Fig 4.3.

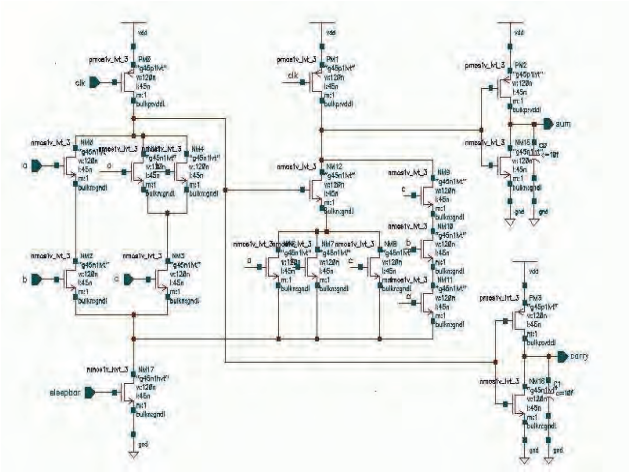

Fig 4.1 Single bit full adder schematic circuit

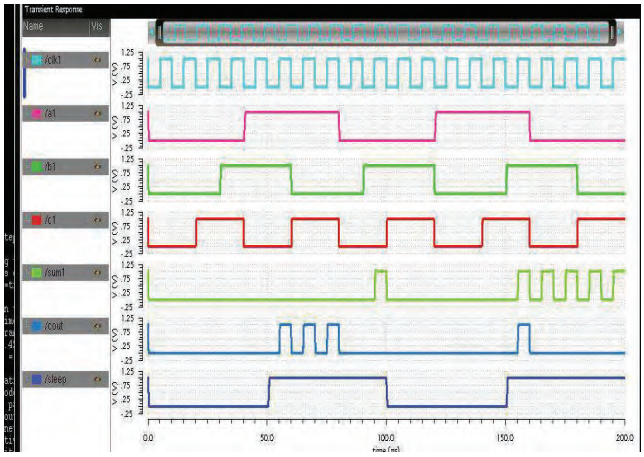

Fig 4.2 Single bit full adder simulation (input-output)

A 8-bit Schematic TSPC full adder is shown below, the design has two 4-bit adders and a carry. Carry is propagated from one 4-bit adder to another 4-bit adder.

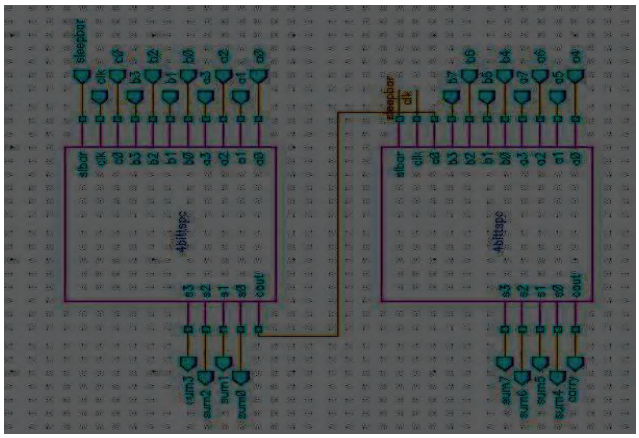

Fig 4.3 Eight bit adder TSPC schematic using two 4 bit adders

The analysis for power dissipation, Leakage power and delay are performed. The Table-1 shows the delay statistics and comparision between CMOS and MTCMOS technology for TSPC adder[6]. TSPC adder Power and Leakage power are tabulated in Table-2 for comparision of CMOS and MTCMOS technology.

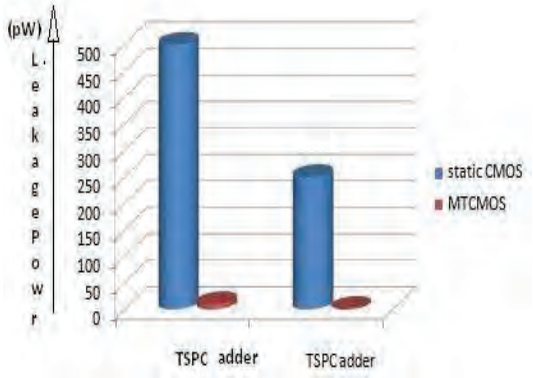

Fig 4.4 Leakage power comparison for CMOS and MTCMOS logic

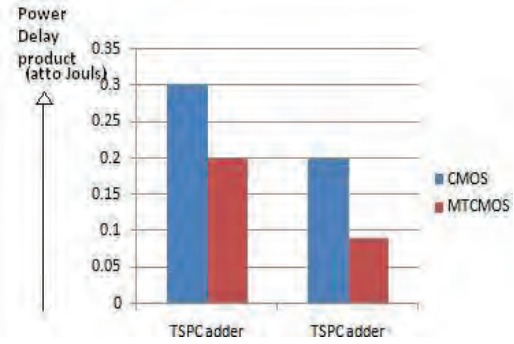

Fig 4.5 Power delay product comparison for CMOS and MTCMOS logic

The Fig 4.4 and Fig 4.5 shows the graphs for Leakage power and Power delay product respectively, with comparison of Static CMOS and MTCMOS technology for TSPC adder, it shows good improvements in MTCMOS TSPC Adders.

Table-1

Comparison of Delay in CMOS and MTCMOS technology for TSPC adder

ADDER	Delay(pS)
CMOS-TSPC Adder	1430(existed)
MTCMOS-TSPC Adder	23.1(Proposed)

Table-2

Comparison of Power and Leakage power in CMOS and MTCMOS technology for TSPC Adder

ADDER	Average Power Dissipation (nW)	Leakage Power (pW)
CMOS-TSPC	1230(existed)	1452 (existed)
MTCMOS-TSPC	603.5(Proposed)	384.5(Proposed)

V. CONCLUSIONS

The 8-bit Ripple carry TSPC adder is designed by using MTCMOS logic and is simulated successfully using 45nm technology. The power dissipation, leakage power and delay are evaluated and compared. The proposed design shows more leakage power reduction. The leakage power is reduced by 96% to 99% in standby mode as

compared to the existing design[4]. The average power dissipation is also minimized. The active mode power dissipation 603.5nW(very less compared to existing design) is achieved with the help of single sleep transistor MTCMOS technology.

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A Novel Approach for Spectrum Sensing with Effect of Radiation

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Abstract—**In Orthogonal Frequency Division Multiplexing (OFDM) large serial data can be converted into parallel data stream. Each parallel block can be transmitted with orthogonal carriers. If the spectrum is not utilized effectively then more number of carriers can be used in wireless applications, but increasing the carriers leads to radiation effect in environment. To reduce the radiation effect, spectrum should be effectively utilized. Effective utilization of electromagnetic spectrum for the unlicensed users to use the licensed spectrum, white spaces i.e. unused frequency bands need to be detected by dynamic spectrum access in Cognitive Radio(CR) .In this paper two spectrum sensing techniques are proposed ,they are energy detection with Wavelet transform and Cyclostationarity sensing.**

Index Terms—**: Spectrum Sensing, radiation, CR and OFDM.**

I. INTRODUCTION

Day by day wireless devices and applications are increased, but the availability of Electro Magnetic spectrum is a limited natural resource. As per Federal Communications Commission (FCC) spectrum access and radiation effect are more significant problem than physical scarcity of spectrum [5]. Radiation effect can be measured by Specific Absorption Rate (SAR) in mobile communication. Subscribers can be seen the SAR value in the standard mobile station (mobile hand set) by *#07# command. While designing mobile handsets, manufactures are always trying to keep the SAR value less than 1.6 Watt/Kg in European countries to avoid radiation[9][11]. This value is different for different countries .To measure SAR value, mobile is tested with some conditions where the mobile is kept near to the user in the presence of base station. The actual SAR values are usually well below those stated below. The maximum SAR for this model as per the compliance standard and the conditions which it was recorded were-Head SAR=0.376W/Kg. In personal communication, CR is built on Software Defined Radio (SDR) which is a robust enhance technology for multi service, reconfigurable and, reprogrammable software. The goal of CR network or wireless node changes its transmission or reception parameters to communicate efficiently anywhere, anytime for avoiding interference with licensed or unlicensed users with efficient utilization of the radio spectrum[7][8]. It uses the methodology of sensing and learning from the environment and adapting to statistical variations in real time. CR is like feedback communication systems which is used to provide forward and backward link between transmitter and receiver .CR Concept was first developed by Defense Advance Research Products Agency (DARPA) scientist, Dr. Joseph Mitola which leads to concept of IEEE 802.22, which is used for wireless Regional Area Network (WRAN) for white space in Television Frequency Spectrum with no interference. In case TV applications of 700MHz [3] band IEEE 802.22.1 is not effective because interference is harmful. To reduce this interference IEEE802.22.2 is recommended [4].

In wireless communication system an efficient use of frequency spectrum can be achieved by radio network which is called Cognitive Radio network. It is an intelligent multi user communication system with following abilities.

- Each user receiver continuously sense the surrounding environment.
- Observe the environment and adapt to it in response.
- Multiple users can Communicate can through a self-organizing manner.

The characteristics of CR

- Flexibility
- Reconfigurability
- Awareness
- Adaptability
- Intelligence

In order to achieve these characteristics CR is modify and access the radio spectrum without causing excessive interference to the primary users and allocates spectrum to the secondary users. The allocation of spectrum of cognitive radio cycle is shown in Fig.1. This includes Sensing of spectrum, Analysis of spectrum and Decision making spectrum. Sensing of spectrum is to detect the unused spectrum holes (white holes). Based on these holes, it is possible for channels to target without collision. Spectrum can be shared by two methods such as cooperative and non-cooperative [1] [3].

Spectrum can be analyzed through the spectrum holes and it allocates the required band to user. While analysis the spectrum holes the following parameters are analyzed. Those are Path loss, Interference, Wireless link errors and Link layer delay.

Spectrum decision depends on Quality of Service (QoS) for secondary users with the parameters Data rate, Acceptable error rate and Delay time etc.

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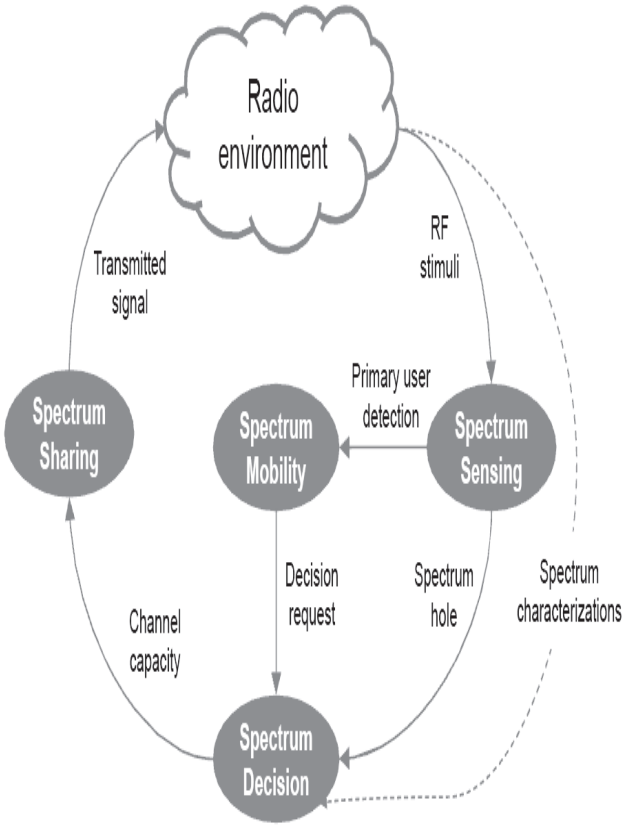

Figure 1.Cognitive radio Cycle.

In this paper various methods of spectrum sensing are shown in Fig 2. We start by introducing the methods of spectrum sensing methods for CR network in section II, Energy detection based Wavelet Packet transform sensing in section III, Section IV Cyclostationarity sensing and Section V simulation results and finally our conclusions are presented**.**

II. SENSING OF SPECTRUM

In this paper, the main focus is sensing of spectrum in CR network. Spectrum sensing can be obtained by using of existence of primary users on a geographical area and database, and by using beacons or local spectrum sensing at CR. Sensing methods not only measures the spectral content, energy over radio frequency spectrum [5][7] but also determines signals occupied in the frequency spectrum including the modulation and carrier frequency. Basically sensing are two methods like cooperative and non cooperative or signal processing techniques shown in Fig2. For CR network, sensing of spectrum requires large dynamic range with high resolution Analog to Digital Converters (ADCs), very high sampling rate and high speed signal processers. While sensing the spectrum the following parameters are to be considered [10].

- Detecting Spread Spectrum Primary Users
- Sensing Duration and Frequency
- Detecting Spread Spectrum Primary Users

A. Principle of sensing of spectrum

Fig. 3 shows the principle of the sensing of spectrum. The figure shows that to protect PU transmission, CR Transmitter is required to perform spectrum sensing to check whether there is any active PU receiver in the coverage of CR Transmitter. If there is any primary user transmission in the coverage of CR Transmitter, then CR Transmitter cannot transmit at that time because it will cause interference to the primary user transmission.

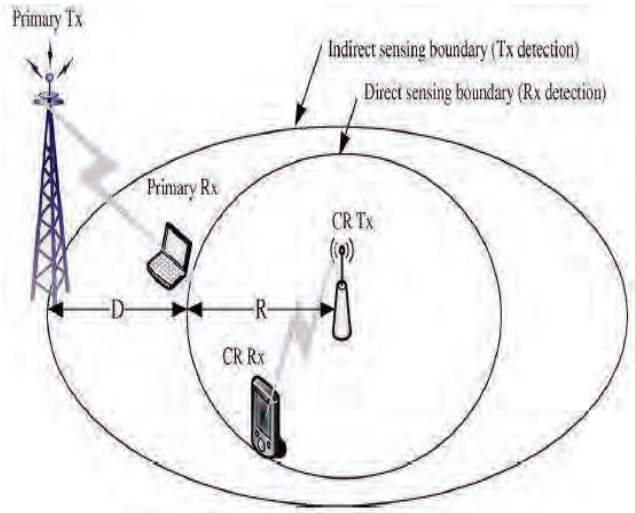

Figure 2. Principle of sensing of spectrum

B.. various methods of sensing spectrum

The main goal of CR network is to detect the spectrum holes without causing interference to the Primary Users (PU) and assign to the Secondary Users (SU). Spectrum sensing can be broadly classified into three major types as shown in Fig.2, non cooperative or transmitter detection, cooperative sensing and interference based sensing[10][11].

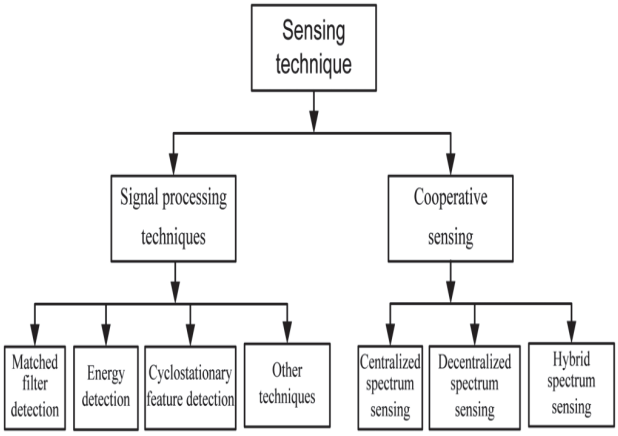

Figure 3. Various methods of sensing spectrum.

Sensing of spectrum plays major role in the cognitive cycle as shown in Fig 1. To improve the sensing of spectrum performance in CR two methods are used, one

cooperative and non cooperative, In Cooperative CR sensors can sense the multiple channels simultaneously and share their sensing information to SU. Cooperative sensing is of three types as shown in Fig. 2. centralized, decentralized and hybrid [7].

In centralized sensing of spectrum each CR sensor senses the spectrum locally and independently making a decision whether the PU's signal is present or absent on a particular channel. This information is passed through the centrally located server or cluster head and takes the decision to infer the absence or presence of the PU. Whenever a CR wireless sensor wants to send data, it requests channel information to the central cooperator [9].

In decentralized cooperative sensing the information can be shared by intra-cluster to other clusters and makes the decision based on demand. In this there is no central control independently take the decision. But it requires a periodic update on the spectrum information table, hence requires more storage and computation [6].

In hybrid cooperation, CR wireless sensors share the information among all sensors in the network. The challenge of CR wireless sensor is computation complexity and allocating resources [8].

In this paper, each radio senses itself about the channel information to know the channel status like idle or busy in noncooperative sensing spectrum method. In cooperative method, CR sensing data with others and use the outcome sensing of others. The detection of PU is depended on the primary transmitter detection. In this approach filter matching is necessary. Due to the low computation complexity and implementation, the energy detection method is most fabulous method. In this approach receiver does not require any knowledge on the PU data. Based on the signal and noise floor comparison, the original signal detected by threshold detector, where choosing the threshold value is key role in this method. The system performance mainly depends on signal to noise ratio value, if the value of SNR is low then, It tries to increase the value of SNR by varying system parameters. While measuring the threshold value two parameters are needed [12][13]. They are Pd (probability correct detection) and Pf (probability false detection) these play critical role in sensing of spectrum.

III. WAVELET PACKET TRANSFORM

Wavelet transform has become more popular in signal processing because it gives signal information in time-frequency. In communication, noise component is having high frequency and signal component is having low frequency. The wavelet transform decomposes a signal into approximation representation that shows signal details and trends as a function of time. Thresholding is the simple method to remove the noise and reconstruct the signal is reducing the size of coefficient detail. These coefficients cannot be zero because it contains original signal information. The two popular methods to reduce the noise are hard and soft thresholding. The principle in Wavelet Packet Transform (WPT) is approximate both high and low pass sub-bands at all scales in the filter bank approximation and implementation. Hence this method is suitable for non-stationary time variable signal to identify the signal information in both high and low frequency bands. The decomposition tree is shown in Fig 4. Signal S to be combination of as A1 + AAD3 + DAD3 + DD2.This combination of representation is not possible with general wavelet but feasible made with WPT [5].

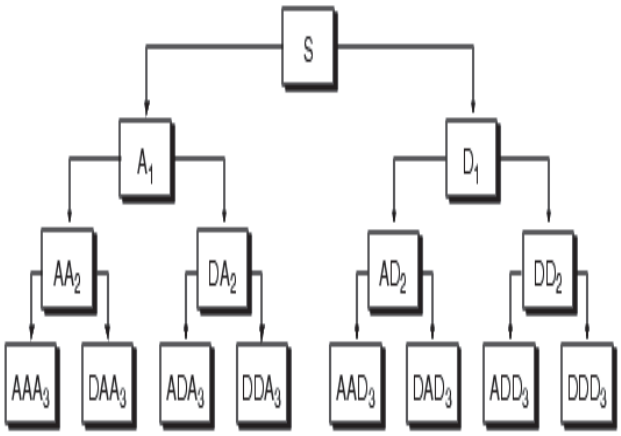

Figure. 4 Wavelet packet decomposition tree

C) Energy Detection Model based on WPT

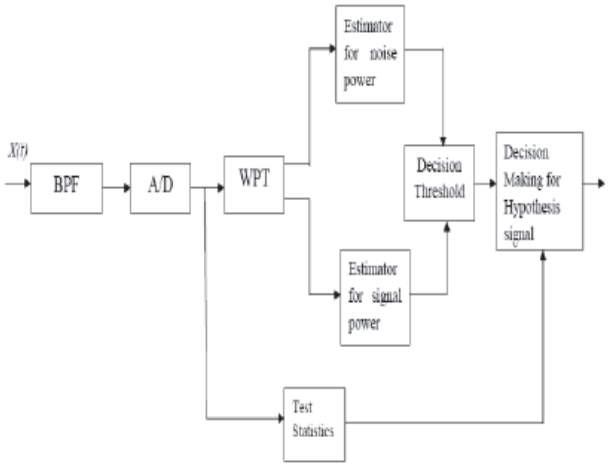

Figure 5 .Block Diagram of energy detection based on WPT

Energy detection based on WPT block diagram is shown in fig 5. Band Pass Filter (BPF) removes the unwanted frequencies and selects the frequencies of bandwidth W Hz then passed through Analog to Digital Converter (A/D) coverts into digital signal consists of both signal and noise x(n).

$$x(n) = s(n) + w(n) \quad n = 0,1 \ldots .N-1 \quad ---(1)$$

Where s (n) is the PU signal with zero mean and variance σ_s^2

W (n) is AWGN with zero mean and variance σ_w^2

If Spectrum can be used by PU then s(n) ≠ 0 otherwise s (n) = 0.Digital signal x(n) can be processed as follows first x(n) is sent to Wavelet Packet transform

(WPT) to estimate current noise power (σ_w^2) and signal power (σ_s^2) calculate the energy of x(n) is decomposed for a certain level related to the resolution required and then is reconstructed by wavelet packet decomposition coefficients. And hence the noise power and reconstructed signal power is estimated [9][10]. If $X > \gamma^*$, we can make a decision that the channel is occupied by one PU or more. Otherwise, the channel is vacant, and SUs could make use of the channel at this moment.

IV. CYCLOSTATIONARITY SPECTRUM SENSING

In energy based detection first decision about the signal contains noise and estimates it. Where as in case of sensing of spectrum using Cyclostationarity is unused or hidden frequencies (called cyclic frequencies) exits in modulation, shifting in frequency, spreading codes and pulse shaping in communication systems. These frequencies can be detected by using mathematical tool such as cyclic autocorrelation and the spectral correlation function. But computational complexity is more in the Cyclostationarity analysis operations due to the nature of the estimation as shown below fig 6.

Figure 6. Cyclostationarity Feature Detector

V. SIMULATION RESULTS

In this paper all the simulations are done in MatLab. First simulate P_d verses different values of SNR using WPT for different samples as shown in Fig 7.and for the same use WPT under different wavelets as shown in Fig8. Finally simulation is done by Cyclostationarity sensing method with QPSK modulation as shown in Fig 9.

In WPT based energy detection the spectrum can be sensed by different sample values had simulated as shown in fig 7. As sample number N is large then P_d is close to 1 .so that better sensing has to be done for only large values of N. But as N increases SAR value increases. The simulation algorithm steps are as follows.

- random signal is generated and add the noise
- The signal is added with AWGN signal is obtained whose WPT is finding out.
- Variance is calculated based on level of threshold.
- Plot the graph between Pd vs. SNR using WPT.

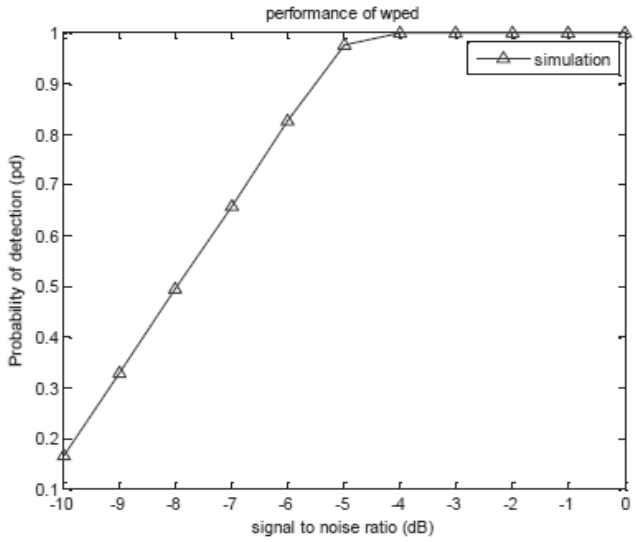

Figure 7. Simulation of PD vs SNR using WPT under different sample numbers.

Same signal has been simulated for different wavelets used for energy detection based sensing is shown in Fig 8 .In this paper the simulation results shows the db2 wavelet. It gives less error for decomposition and reconstruction of the signal.

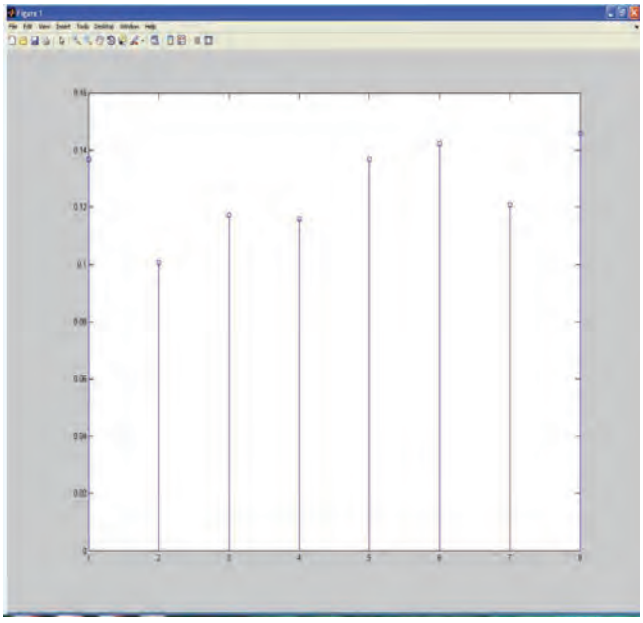

Figure 8. Simulation of PD vs SNR using WPT under different wavelets.

D. Simulation of Cyclostationarity sensing

In energy based sensing is based on P_d and Pf value under signal is noisy environment. Where as in Cyclostationarity the signal is transmitted with Quadrature Phase Shift Keying (QPSK) modulated with a carrier frequency of 200Hz, we get two peaks at 400Hz. These peaks signifies that the PU uses the QPSK and the reason for getting peaks at double the carrier frequency is autocorrelation of the received signal.

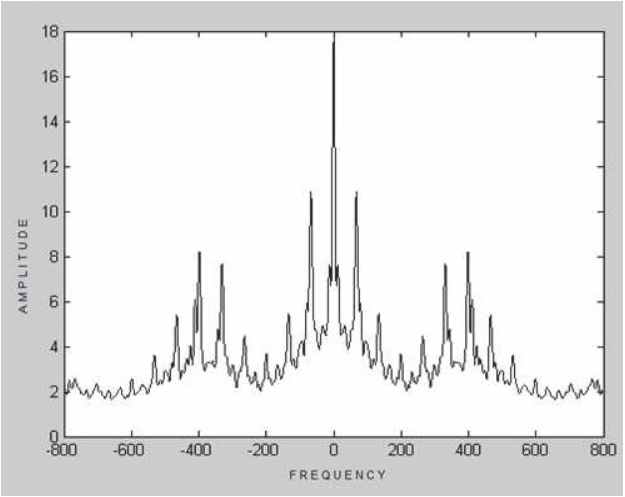

Figure 9. Simulation of Cyclostationarity spectrum sensing with QPSK modulation

VI CONCLUSIONS

WPT based energy spectrum sensing is best method in noisy environment compared to the conventional methods. In this paper the probability is closely reached to the value 1 as the number samples are increased at low SNR Cyclostationarity sensing is good method compared with the regular method. As we utilize the spectrum efficiently then automatically number of carriers are reduced which results in reduced radiation effect.

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An Effective Method for Implementing 64-bit MAC using Wallace Tree Multiplier on FPGA through Chip Scope Pro

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***Abstract*—Most of the Digital Circuit Designers are failing at programming the FPGA when the net list of design exceeds specified NETs of the desired FPGA. This paper presents the simplest way to programming the FPGA is not only programming, but also testing Circuit Under Test (CUT) by applying all possible test vectors manually through the keyboard. Presently running On-Board values can also be viewed on the monitor. If designers are new to FPGA design, this paper will help them to learn some of the debugging options.**

***Index Terms*- Chip scope pro, ILA core, Vio core, ICON.**

I. INTRODUCTION

The MAC (Multiplier-Accumulator) unit is made up of multiplier and an accumulator. This contains the sum of previous successive products. The multiplier used in this is a Wallace Tree Multiplier and the adder is Carry Save Adder (CSA).MAC inputs are obtained from the memory location and given to the multiplier block. Since it is a 64 bit MAC [1] unit, multiplier inputs are 64 bits. Therefore the MAC unit requires 128 bit adder and 129 bit accumulator.

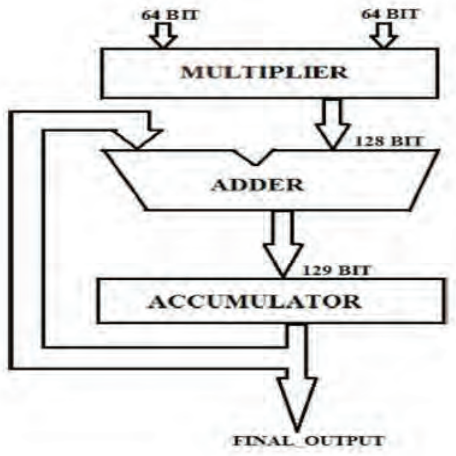

Figure 1.1 64-bit MAC Block Diagram

With the recent expeditious advances in communication systems and multimedia, real time signal processing like audio, video and image signal processing, large-capacity data processing are increasingly being required. In computing, generally the multiply–accumulate operation is a rarely used step. It computes the product of two numbers and adds that product to an accumulator. The hardware unit which performs the operation of both multiply and accumulates known as a multiplier–accumulator (MAC, or MAC unit) the operation itself is called a MAC or MAC operation.

The principle of multiplication of the MAC unit is based on twofold method, i.e. it evaluates partial products (pp) and the summing process takes place with shift partial products.

The least significant bit (the right most bit) of the multiplier is then multiplied with the multiplicand bit, corresponding partial products are stored in a register. The same process is repeated until the most significant bit (left most bit) is reached. The process of multiplication is shown in fig. 1.2.

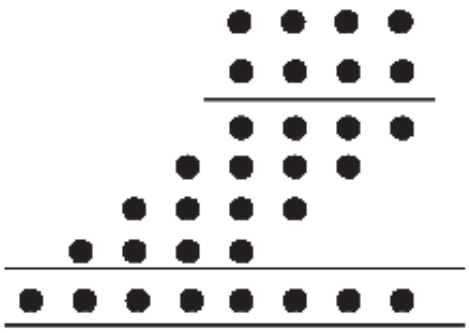

Figure 1.2 Basic Multiplication

A MAC unit consists of a multiplier and an accumulator containing the sum of the previous successive

products. The multiplier used is Wallace Tree Multiplier [2] and the adder used is Carry Save Adder [3]. The MAC inputs are obtained from the memory location and given to the multiplier block.

The multiplier used in this is a Wallace Tree Multiplier. It is an efficient multiplier with reduced complexity as compared with the conventional multiplier. The power consumption of Wallace Tree Multiplier is very less. The multiplication process using Wallace Tree Multiplier is shown in fig 1.3.

It uses a tree structure and reduces the number of additions in the critical path to O (log n) rather than O (n). The number of partial products in Wallace Tree Multiplier are reduced by the use of half and full adders in the design. It also uses compressors to reduce the complexity.

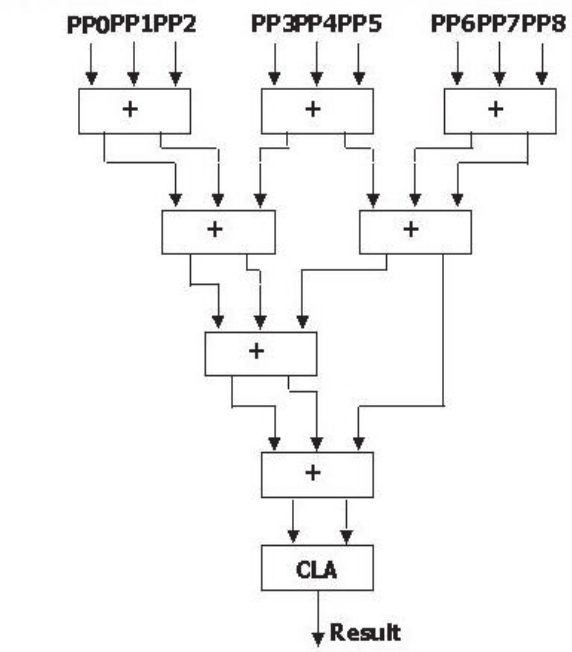

Figure1.3. Wallace tree multiplier

II. Need of Chip Scope Pro

'Chip Scope' is a set of tools designed by Xilinx that allows probing the signals, i.e., testing the signals of design inside an FPGA, much as would do with a logic analyzer. For example, while design is running on the FPGA, the designers can trigger when required events are taking place and can view any internal signal of the design. Since, the 'Chip Scope' analyzer's logic is implemented in the FPGA, it has some important limitations.

The sample memory of the analyzer is confined by the memory resources of the FPGA. In a design that uses much of the FPGA's memory, there may not be much of memory left for the 'Chip Scope' cores [4]. Also, 'Chip Scope' cannot sample as quickly as external logic analyzer. Generally, the Chip Scope sampling rate will be the same as the design's clock frequency. It is therefore not possible to detect glitches. In order to use the Chip Scope internal logic analyzer in an existing design project, first generate the Chip Scope core modules, which perform the trigger and wave form capturing functionality on the FPGA. Afterwards, initiate these cores in Verilog or VHDL code, and connect those modules to the signals that are to be monitored. The complete design is then recompiled, instead of loading the resulting ".bit" file onto the FPGA using iMAPCT. The 'chip scope' analyzer also provides the interface for setting the trigger criteria for the Chip Scope cores, and displays the waveforms recorded by those cores.

III. Core Generator Flow

There are certain rules and regulations to add the cores for a design. These rules and regulations are to be properly maintained, to configure the design to FPGA board.

They are

1. Configuring the design
2. Creating cores
3. Adding the cores
4. Configuring.

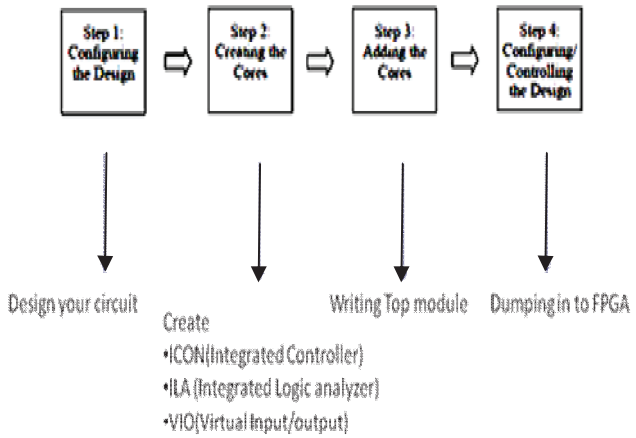

Figure3.1 Core generation flow

Step1: Configuring the design: Designer should complete the circuit with all aspects like power optimization, area optimization.

Step2: Creating cores: Like ILA, VIO& ICON cores need to be created. The creation of core of a design particularly depends on the number of inputs and outputs.

Step3: Adding cores: Top level program in structural manner either Verilog or VHDL language.

Step4: Configuring: i.e. programming FPGA and verifying.

IV. IDEA BEHIND THE CHIPSCOPE PRO

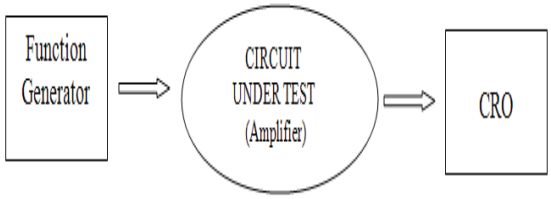

Figure 4.1 Idea behind the chip scope pro

In case of hardware, the designer tries to check the circuitry, whether it meets design constraints or not with the help of FG (Function Generator) and CRO (Cathode Ray Oscilloscope).

In case of software(VHDL or Verilog), same digital circuits can be tested using 'Chip Scope Pro' irrespective of the number of inputs and outputs of the design. This can be done by adding cores to the design and that cores are ILA (Integrated Logic Analyzer), VIO (Virtual Logic Input/output) & ICON (Integrated Controller).

V. DESIGN AND IMPLEMENTATION OF CORE GENERIC FLOW

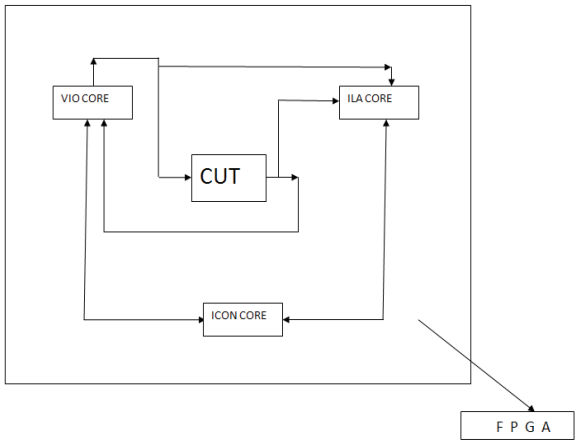

Figure 5.1 Arrangement of added cores to FPGA

From the steps mentioned above, first there is a need to add the core to design circuitry or CUT (Circuit Under Test).The cores are ILA (Integrated Logic Analyzer), VIO (Virtual Logic Input/output) and ICON (Integrated Controller). After that, writing the top level module either in Verilog or VHDL [5][6].Fig.5.1shows the basic idea of writing a top level module to the circuit.

VI. ANALYSIS PROCEDURE

ICON core insertion:

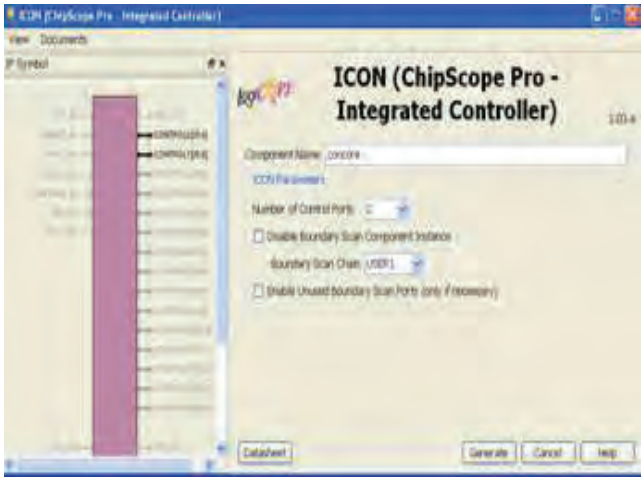

Figure 6.1 ICON Core insertion

Usually controller is useful for controlling the design. Here the ICON is also working same as Controller in general design. Here it controls 15 numbers of cores, whereas this MAC unit requires two control signals with each 36 bits wide.

VIO core insertion:

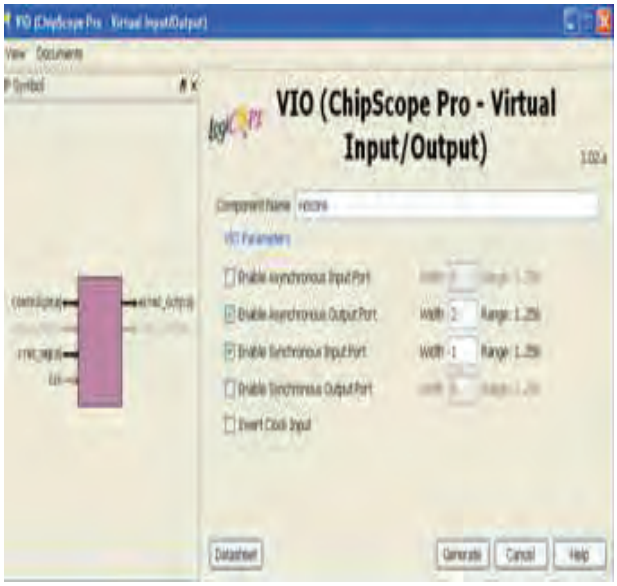

Figure 6.2 VIO Core Insertion

It is basically used for generating Inputs to MAC unit. Sometimes called it as test vector generator for the circuit under test. The total number of inputs required for this core is 129 and possible generation of test vectors is 128.These 128 TV's are fed to the input of 64-bit MAC unit.

ILA core insertion

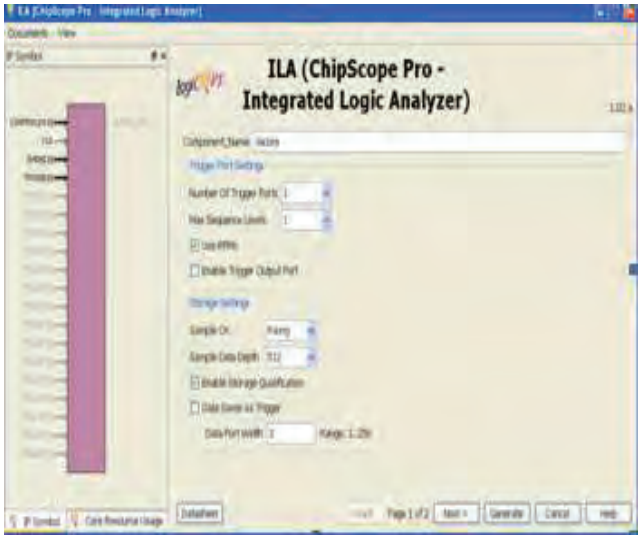

Figure 6.3 ILA Core insertion

In the general case, it can simply act as a CRO. It means that, it takes all possible inputs and outputs of the 64-bit MAC.

In this circuit it analyzes 129-bit of output with corresponding 128-bit input.

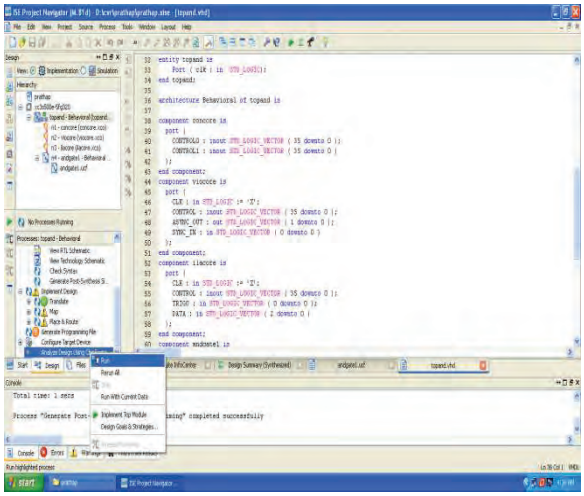

Figure 6.4 Simulation step for analyzing through Chip scope

Figure 6.5 Programming of FPGA

After adding cores to the MAC unit ".bit" file is needed in order to program it to the FPGA by clicking on "Analyze using Chip scope" as shown in Fig.6.4. A ".bit" file is generated (where as traditional iMPAT method takes many more steps for generating ".bit" file.) and one pop-up window is opened as shown in fig.6.5. With this programming is done.

VII. RESULT

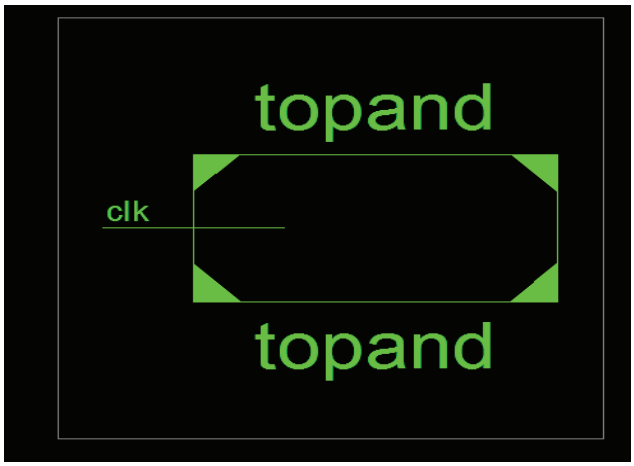

Figure 7.1 MAC unit Top module.

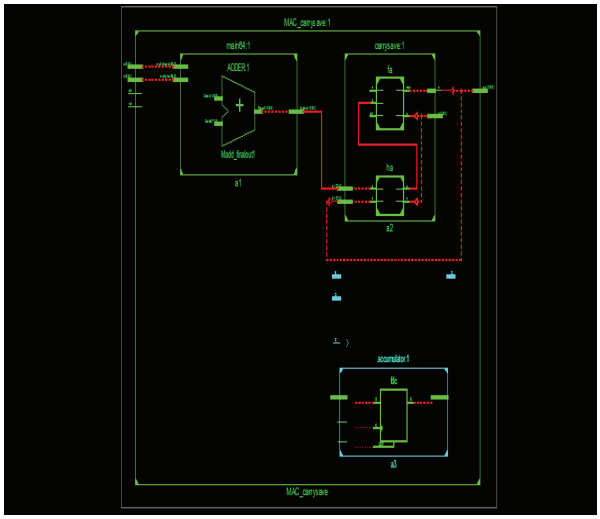

Figure 7.2 RTL Schematic of MAC unit before adding the cores

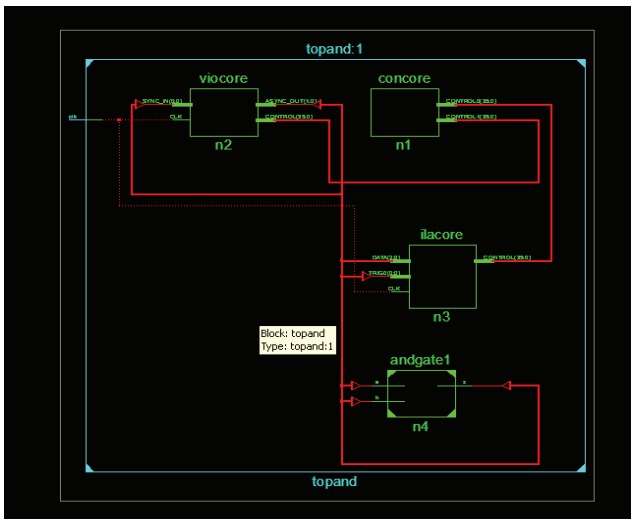

Figure 7.3 RTL Schematic of MAC unit after adding cores.

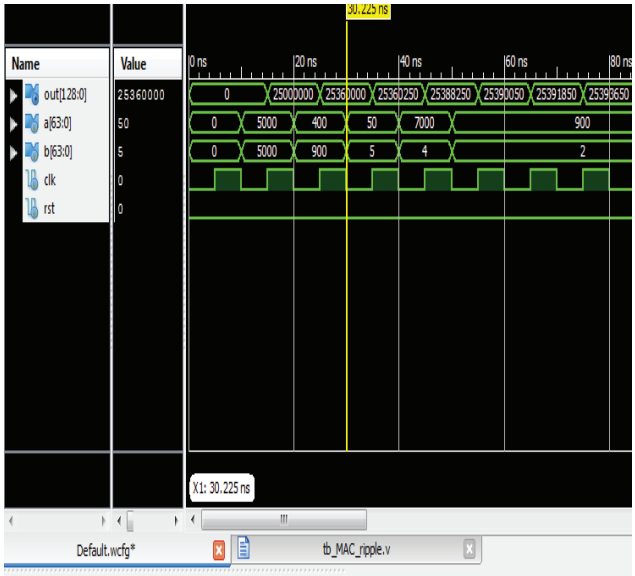

Figure 7.4 Simulation results of MAC unit before programming.

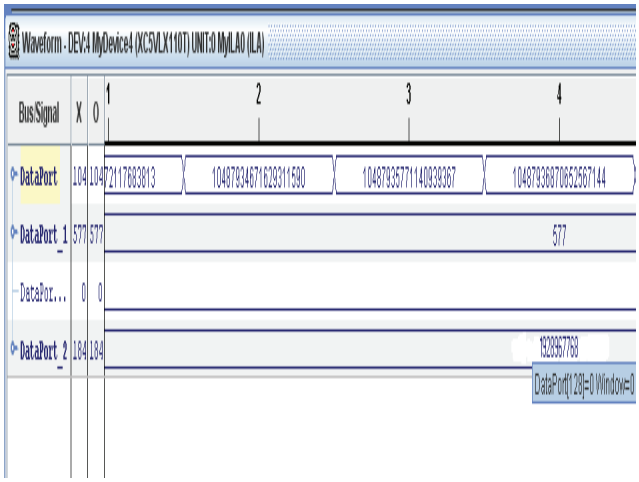

Figure 7.5 Simulation results of MAC unit after programming using chip scope pro.

VIII CONCLUSIONS

It is concluded that, using 'chip scope pro' one can analyze any circuit with any number of inputs. With Spartan 3E FPGA only four signals can be analyzed, but by interfacing with 'Chip scope pro' it can be increased up to 256. Similarly, Virtex 5 ranges to 1024 from its 8 pins.

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Implementation of Various Spectrum Sensing Algorithms in Cognitive Radio Network

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Abstract— **Spectrum sensing is a crucial task in Cognitive Radio networks. In this network some frequency bands are allocated for primary users. Secondary user can detect the unlicensed spectrum bands which are called white spaces without disturbing the primary user. The Common control channel, Channel estimation, Joint sensing and spectrum access, the location information are the other challenges of CR networks. To reuse the spectrum, spectrum sensing is necessary and several techniques available for spectrum sensing based on band of interest [2]. In this paper, Basis Pursuit(BP) and Orthogonal Matching Pursuit(OMP) algorithms are used for signal reconstruction[1]. All the simulations are carried out using MATLAB.**

IndexTerms- WHT, DCT, DFT, Compressive Sensing, Basis Pursuit and Orthogonal Matching Pursuit(OMP) .

I. INTRODUCTION

Energy detection, Feature detection, Matched filtering, Covariance based detection and Eigenvalue based detection (EBD) methods belong to narrowband sensing. In energy detection, the PU signal energy is obtained in a specific time period of a particular frequency band and it has less computational complexity. The performance of this algorithm can be achieved by Pd (Probability of detection) and Pf (Probability of false alarm). It has poor detection performance under the low SNR which is the major drawback in this scheme.

The feature detection technique is based on the cyclic feature which is originated by the mean and auto correlation of a periodic signal. This algorithm can detect the noise from the signals as the noise is Wide-Sense Stationary. This process separates the desired signal from the noise but it requires long observation time and higher computational complexity.

To increase the output SNR for a certain input signal a matched filter is used which belongs to the linear filter. The major advantage of this scheme is it requires only O(1/SNR) samples to meet a given probability of detection. But it consumes large power.

Covariance based detection is another narrow band spectrum sensing which exploits the inherent correlation in received signals at the CR terminal ensuing from the oversampling of received signal. It does not require any prior information about the PU signal or noise. In this scheme the noise power estimation is not a requisite here as the threshold is related to false alarm probability and number of samples of the received signal at the CR. The better performance would be achieved for highly correlated PU signals while the performance of this detection degrades with the uncorrelated PU signal. To improve the signal quality at the receiver various Compressive sensing techniques are introduced. Table.1 shows the advantages and disadvantages of Energy, Feature, Matched filter and Covariance based Detection Methods.

TABLE 1.

VARIOUS SPECRTUM SENSING SCHEMES COMPARISON

SS scheme	Advantages	Disadvantages
Energy Detection Method	Easy to implement, Low computational complexity	Threshold depends on Noise uncertainties. Non Robust and Low accuracy. Hidden terminal problem is susceptible .
Feature Detection Method	Noise uncertainty. High reliability.	Complex to implement and nonblind.
Matched- filter Detection Method	Less complex and Less susceptible to the hidden terminal problems.	Nonblind, complexity and sensitivity is high
Covariance based Detection Method	High Accuracy, blind,less and computational complexity.	Degrades the performance for uncorrelated PU signals

II .WIDEBAND SPECTRUM SENSING

To sense a bandwidth which exceeds the coherence bandwidth of the channel these techniques are used.. They can be classified into Nyquist rate and Sub-Nyquist wideband sensing techniques. The former one processes digital signals at or above the Nyquist rate, while the latter using the sampling rate below the Nyquist rate.

A. Nyquist Rate Wideband Sensing

To detect the spectral opportunities in Nyquist rate wideband sensing, a standard ADC and DSP algorithms are used. A filter bank approach is a good solution for the multicarrier wideband sensing. The baseband signal can be estimated by using a prototype filter, and other can be obtained by modulating it. In order to locate the singularities and irregular structures of the wideband PSD, the wavelet transform is an attractive mathematical tool, chosen for this scheme [5]. This algorithm works well for the wide range of bandwidth to simultaneously identify all the piecewise smooth sub bands, without having prior information about the number of sub bands within the band of interest.

B. Sub Nyquist Rate Wideband Sensing

If the sampling rate is less than the Nyquist rate and detecting spectral opportunities in the Nyquist wideband sensing, they can be categorized into Wideband CS and Wideband Multi-Channel Sub-Nyquist sensing. Compressive Sensing belongs to this category. CS can be used to recover the wideband signal when the spectrum is sparse due to its low utilization and capitalizing the sparseness. In CS a finite-length time-variant signal x(t) can be represented by

$$x(t) = \sum_{i=1}^{N} b_i \psi_i(t) = \psi\, b \qquad (1)$$

where b_i indicates the basis coefficients of the sparse signal x(t).

In sparse signals, x can be expressed as a weighted sum of S orthonormal basis functions, with $S << N$ and it can be obtained from equation (1). Those are significant Number of NonZero (NNZ) elements, while the remaining (N−S) of values gives less significant elements or zeros. The output y can be written as

$$y = \varphi\, x = \varphi\, \psi\, b = \Theta\, b \qquad (2)$$

Where $\Theta = \phi\psi$ is a matrix of size M X N and the size of y is smaller than that of x, and then it provides infinite number of solutions. The recovery of x can be obtained with a measurement matrix, Φ and y by solving the l1 -norm minimization problem is given by

$$\hat{b} = \arg_b \min \|b\| 1 such that\ \Theta\, b = y \qquad (3)$$

This is a convex optimization problem which is solved by the Basis Pursuit (BP), an iterative greedy algorithm, etc. The advantage of this scheme is robust to noise and can afford less number of samples.

C. Measurement Matrix of CS Recovery

To make M measurements from the signal x with length-N could be reconstructed by its sparse coefficient vector s. The reconstruction will not be possible if the measurement process damages the data in x. Hence, this process is linear and has an infinite no. of solutions with fewer equations than unknowns.

III . VARIOUS TRANSFORMATION TECHNIQUES

A. Walsh - Hadamard Transform Coding

A Walsh matrix is a square matrix, with a power of 2 dimensions, the elements of the matrix are +1 or 1,and the dot product of any two rows (or columns) is zero. Each row of a matrix corresponds to a Walsh function. Hadamard is a computationally simpler than the Fourier transform, since it requires no complex arithmetic operations. These operations were extremely time intensive on the small computers[3]. We have

$$y = Hx; \qquad (4)$$

$$x = Hy; \qquad (5)$$

From equations (4) and (5) x denotes the input, y is the output, and H is the Hadamard transform matrix which is symmetric and self-inverse:

$$H^T = H = H^{-1} \qquad (6)$$

The transform matrix of the 2 X 2-Hadamard transform is given by

$$H^{(2)} = \frac{1}{\sqrt{2}} \begin{bmatrix} H^n & H^n \\ H^n & -H^n \end{bmatrix}$$

The Walsh-Hadamard transform can be obtained by rearranging the basis vectors according to the number of zero crossings.

B. Discrete Cosine Transform

In DCT a data sequence is represented by a sum of cosine functions. It is widely used in science and engineering, audio and image compression techniques. It is expressed in the following four types of DCTs

DCT-I

$$C_k^{\ I}(n) = \frac{2}{\sqrt{N}} \gamma_k \gamma_n \cos(kn\pi/N),\ k, n = 0,1,2,.....N$$

DCT-II

$$C_k^{\ II}(n) = \frac{2}{\sqrt{N}} \gamma_k \cos\frac{k(n+\frac{1}{2})\pi}{N},\ k, n = 0,1,2,.....N$$

DCT-III

$$C_k^{\ III}(n) = \frac{2}{\sqrt{N}} \gamma_n \cos\frac{(k+\frac{1}{2})n\pi}{N},\ k, n = 0,1,2,.....N$$

DCT-IV

$$C_{k^{IV}}(n) = \frac{2}{\sqrt{N}} \cos\left(\frac{(k+12)(n+12)\pi}{N}\right), k = 0,1,2,....N \qquad (7)$$

The coefficients $C_k(n)$ are given by the equation

$$C_k(n) = \left[C_k(0), C_k(1).....\right]^T \qquad (8)$$

let us consider the forward and inverse DCT-II:

$$X_{c_{II}}(k) = \sum_{n=0}^{N-1} x(n)\, C_{k_{II}}(n)$$

$$= \gamma_k \sqrt{\frac{2}{N}} \sum_{n=0}^{N-1} x(n) \cos\left(\frac{k(n+\frac{1}{2})\pi}{N} \right) \quad (9)$$

$$x(n) = \sum_{k=0}^{N-1} X_{c_{II}}(k)\, C_{k_{II}}(n)$$

$$= \frac{\sqrt{2}}{N} \sum_{k=0}^{N-1} X_{c_{II}}(k)\, \gamma_k \cos\left(\frac{k(n+\frac{1}{2})\pi}{N} \right) \quad (10)$$

The DCT-II is of major importance in signal coding because its correlation coefficient is close to one.

C. Discrete Fourier Transform

The transform pair of the Discrete Fourier Transform (DFT) is defined as

$$X_k = \sum_{n=0}^{N-1} x(n)\, W_N^{nk}$$

$$x(n) = \frac{1}{N} \sum_{k=0}^{N-1} X(k)\, W_{N^{-nk}} \quad (11)$$

$$where \quad W_N = e^{-j\frac{2\pi}{N}}$$

Due to the periodicity of the basis functions, the DFT of a periodic signal with period N.

$$x = \begin{bmatrix} x(0) \\ x(1) \\ : \\ x(N-1) \end{bmatrix} \quad X = \begin{bmatrix} X(0) \\ X(1) \\ : \\ X(N-1) \end{bmatrix}$$

$$W = \left[W_N^{nk} \right]$$

the above relationships can also be expressed as

$$X = Wx \leftrightarrow x = \frac{1}{N} W^H X \quad (12)$$

It is observed from the above equation that W is orthogonal, but not orthonormal.

The DFT can be normalized as follows:

$$\alpha = \phi^H x \leftrightarrow x = \phi\alpha$$

$$where \quad \varphi = \frac{1}{\sqrt{N}} W^H \quad (13)$$

IV. DIFFERENT SCHEMES OF CS RECOVERY

CS Recovery schemes can be used for spectral estimation. Instead of Fourier representation Wavelets dictionary gives a better result. This dictionary contains Steerable Wavelets, Segmented Wavelets, Multi-scale Gabor dictionaries, Wavelet Packets etc. The decomposition of a signal s can be written as

$$s = \sum_{\gamma \in \Gamma} \alpha_\gamma \varphi_\gamma \quad (14)$$

or an approximate decomposition

$$s = \sum_{i=1}^{m} \alpha_{\gamma i} \varphi_{\gamma i} + R^{(m)} \quad (15)$$

where $R_{(m)}$ is a residual. The recovery signal representation decomposes into pure tones, bumps, chirps etc. depending on the dictionary.

A. Basis Pursuit Algorithm

The principle behind Basis Pursuit (BP) is decomposition of a signal into an optimal superposition of dictionary elements [4]. BP is used in ill-posed systems, total variation and multiscale edge denoising. It can be used with noisy data by solving an optimization problem measure with an l1 norm of coefficients. Among the many possible solutions to $\phi\alpha = s$, they pick one whose coefficients have the minimum l1 norm.

$$\min \|\alpha\|_1 \; subject\ to\ \varphi_\alpha = s \quad (16)$$

To deal with the signal at the noise level $\sigma > 0$ it is proposed an approximate decomposition as in equation(16), solving

$$\min \|\varphi_\alpha - s\|_2^2 + \lambda_n \|\alpha\|_1 \quad (17)$$

$$\lambda_n = \sigma\sqrt{2\log(\#D)}$$

with depending on the number of different vectors in the dictionary.

B. Orthogonal Matching Pursuit

Let s be a d-dimensional s-sparse signal. Let $\{x_1, x_2 \ldots\ldots x_N\}$ be a sequence of input vector in

R^d . Those vectors can be used to collect N linear measurements of the signal

$$\langle s, x_1 \rangle, \langle s, x_2 \rangle, \ldots\ldots \langle s, x_N \rangle$$

The procedure of OMP scheme is

1. Initialize the residual, index set and the iteration counter t = 1.
2. Find the index λ_t which solves the optimization problem $\lambda_t = \arg\max_{j=1,\ldots,d} |\langle r_{t-1}, \varphi_j \rangle|$
3. Augment the matrix of chosen atoms.
4. Obtain a new signal estimate by using the equation $x_t = \arg\min_x \|v - \phi_t x\|_2$
5. Calculate the new residual.
6. Increment t, and return to Step 2 if t < m.
7. The estimate $\hat{s}$ in component Λj equals the j[th] component of x_t.

V. SIMULATION RESULTS

In this paper different CS schemes have been discussed for sparse signal acquisition. Most of the CS based signal acquisition schemes require a measurement matrix based on sparsity. In this paper, the performance analysis of WHT, DCT and DFT transform coding techniques are compared. Usually, DFT and DCT transform coded measurement matrix provides the similar results, while the comparison between WHT and DCT transform coded measurement matrix illustrates a very significant result in the wideband sensing algorithm.

We consider, at baseband, a wideband spectrum range [0MHz to 60MHz] containing 30 channels of 2 MHz each. Every channel is occupied by a Primary User (PU) with a digital modulation scheme either 16-PSK or 16-QAM. So, the symbol rate is 2 MHz and number of samples per symbol is 16 and number of symbols in a frame is chosen 512. In a single attempt there are three PUs communicating with the center frequency of 20:7 MHz, 45:3 MHz, 59:5 MHz respectively, while their individual bandwidth is 2 MHz each. Here, we have considered the Nyquist sampling frequency, fs = 128 MHz and the sampling number, N = 8192.We also consider, the received signal at the cognitive terminal is corrupted by the AWGN. The signal to noise ratio of active channels is considered to be 20dB. For CS reconstruction, the chosen compression ratio is varying from 2.5% to 60%. The compressed matrix Φ is Gaussian distributed with zero mean and variance $1/M$ and these matrices allow sparse recovery using l1 minimization. The above transformation techniques are used to form the measurement matrix, Φ and then compares the normalized MSE w.r.t. PSD.

The NMSE(Normalized Mean Square Error) of the PSD is defined by:

$$MSE = E\left\{\frac{\|\hat{s}_x - s_x\|_2^2}{\|s_x\|_2^2}\right\} \quad (18)$$

where s_x denotes the average of the PSD estimates and $\hat{s}_x$ is the average PSD estimate of the reconstructed signal through the compressive sensing from the periodogram of same type. From Figure.1 it is clearly observed that the signal reconstruction quality is better with higher compression ratio M/N .

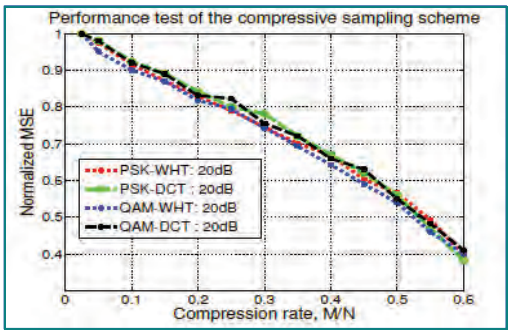

Figure 1. Normalized MSE versus compression rate

In order to compare the DCT and WHT matrices execution time, we consider the compression rate M/N of interest in the range of 2.50%-60%. Figure 1 shows that the WHT matrix executes 30% faster than its DCT counterparts while their detection probability as shown in Fig.2 is comparable.

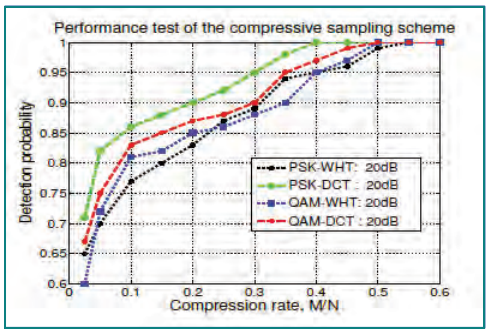

Figure 2. Detection probability versus compression rate

The probability of detection, p_d is defined as:

$$p_d = p_r(N > (\gamma / H_1))$$

$$N = p_r(N > (\gamma / H_1))$$

$$N = S_x(k) = \frac{1}{Q}\sum_{q=1}^{Q}\left|X_q(k)^2\right| \qquad (19)$$

Where $X_q(K)$ is the Fourier transform of the signal $x_q(n)$ and n indicates the sample index with 8 PSD samples in each block.

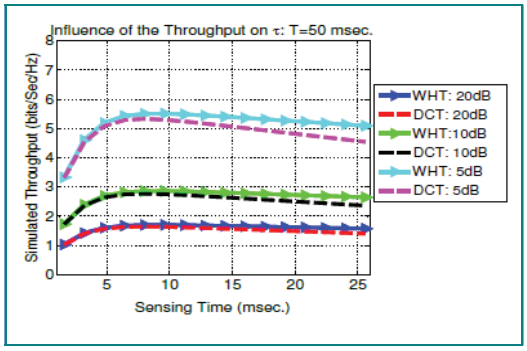

Figure 3. Influence of compression ratio on the detection performance

Where γ is the decision threshold found by fixing the probability of false alarm, Pf = 0.05 and H1 represents the presence of PUs. Fig.3 describes the Pd with various values of compression ratios.

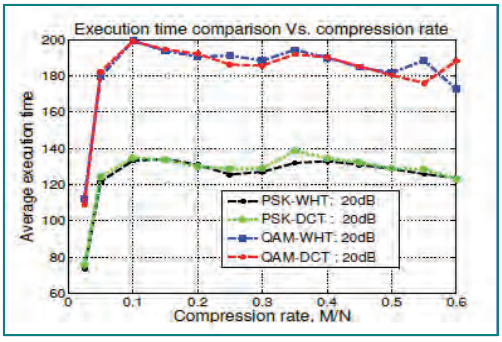

Figure .4. Execution time versus compression rate

Fig.4 shows that the relation between execution time and compression ratio for various modulation techniques.

VI CONCLUSIONS

In this paper various detection schemes are discussed. For signal recovery Basis Pursuit and Orthogonal Matching Pursuit algorithms are used along with Walsh Hadamard, Discrete Cosine and Discrete Fourier Transform techniques. These two techniques give a better result than Energy detection, Feature detection, Matched filter detection and Covariance based detection Methods. This is proved with the help of simulation results. It is concluded that the signal reconstruction quality is better with higher compression ratio. A novel compressive spectrum sensing algorithms can be implemented in future.

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Automatic Cheque Clearance System using MATLAB

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Abstract— **Nowadays Cheque Truncating System (CTS) compliant cheques are used in banks for saving time and reducing effort in depositing cheques. With the development of image processing it is possible to make machines read the documents instead of humans. Applying the image processing technique in the cheque deposition in banks can reduce the human effort, time and also will be cost effective. In this paper, an automatic cheque clearance system is discussed using Optical Character Recognition (OCR) system by feature extraction and pattern recognition concepts in image processing. Using this one, can reduce time, human effort and money in processing of cheques. The algorithms are executed using MATLAB.**

Index Terms— **CTS, OCR, cheque, MATLAB.**

I. INTRODUCTION

Cheque truncation is the process of stopping to send the physical cheque to the drawee branch issued by the drawer branch. Instead of sending the physical cheque, the electronic image of the cheque along with the relevant information like date of presentation, MICR fields and presenting banks etc. is sent to the drawee branch. This process would help to avoid moving the cheques physically across the branches except in some exceptional cases. This would result in reduction of the time required for payment of cheques thus speeding up the process of realization or collection of the cheques [1].

This paper uses the image processing algorithms like feature extraction and pattern recognition for automation and faster clearance of cheques.

A. Different fields of cheque

Cheque is the main document for payment of money from a payee an account or payment to another bank. So it is necessary to know the different fields in a cheque. In general some fields of the cheque are already filled and some fields are given with dotted lines or boxes that have to be filled and signed by the account holder who issues the cheque. All the cheques contain name of the issuing bank and some cheques contain name of the account holder along with account number printed on each leaf of the cheque book. In case these are not given, one has to fill these details in correctly. Let us discuss different fields in the cheque with reference to the sample cheque, shown in figure 1.

The name of the person to whom the money has to be paid is written and has to be spelt correctly close to the "pay". Date must be written properly, the current date for the receiver to be able to receive the payment should be written. At the end of the line from "pay" we will find the words "or bearer". This refers to the person who is carrying the cheque and payment will be made to this person if the cheque does not specify the person whom money has to be paid. It is advisable to cross the "or bearer" printed on the cheque when writing out a cheque to avoid a stolen cheque from being misused.

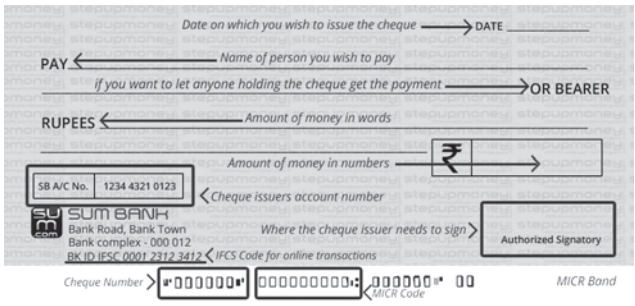

Figure 1: Sample cheque

The payment amount should be written in words next to the printed words on the cheque saying 'Rupees' and the same value should be written in the box beside it in figures. The account holders name is printed at the right bottom of the cheque. Signature has to be made above the field where name is printed. For the purpose of identification each cheque has a different number which is different from bank to bank. The cheque number is normally a six digit number enclosed within inverted commas. The cheque bears a nine digit number called Magnetic Ink Character Recognition code (MICR) which is unique for each branch of a bank in India. The cheque also bears the drawee bank, state, branch and sort code which are a series of numbers appearing next to the cheque number. The cheque may also contain the internal code issued by the bank called transaction id.

II. OPTICAL CHARACTER RECOGNITION

Optical Character Recognition Technology (OCR) is the technology used for converting the scanned documents into machine readable format files. It is not possible to search the content in a scanned document that is stored in the memory of a computer. OCR is the technology which

enables recognizing the characters through an optical mechanism automatically [7]. OCR can recognize both printed text and handwritten text [3]. The performance of the system is dependent on quality of input documents and this OCR is designed to process the documents that contain almost text with little non text clutter. OCR is the process of converting electrical and mechanical forms of scanned images of type written and handwritten into machine text. This machine text is digitized for easy search, to store more compactly and for display online.

OCR technology enables the scanned images to become documents that can be fully searchable with text content that is recognized by the computer. OCR is the process to extract the document information and enter automatically instead of manually entering the information into the electronic database which results in efficient information processing in less time and is more accurate. The block diagram of the OCR is shown in figure 2 [4] [5].

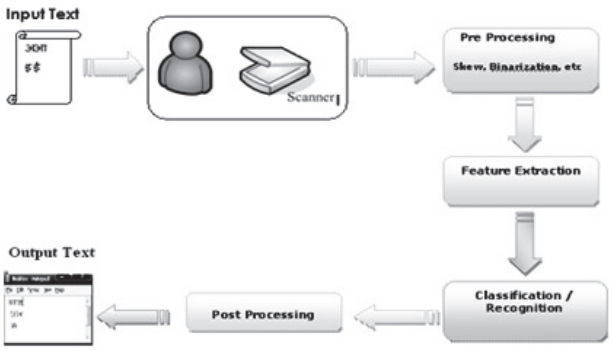

Figure 2: Block Diagram of OCR

The main functional blocks in OCR are Image Acquisition, Pre-processing, Feature Extraction, Pattern Recognition, Post-processing and display. Image acquisition is the process of obtaining text image from the scanner or pre stored files.

A. Scanning:

The scanner contains the camera which captures images and converts original document into digital image. In general original documents are made up of black colored text printed on the white background. Scanning comprises, thresholding which converts digital image as gray scale image. Thresholding is the process of converting multi-level image into bi level image called black and white image. The fixed value is defined in thresholding, if the gray levels are below the threshold level then it identified as black, whereas, if the threshold is above it is identified as white which results in saving memory and computational efforts. The scanner scans the pixels of the text and not the characters. The data may carry some noise while patterns are scanned and digitized. The scanner with low resolution may produce smeared images and touching line segments.

B. Preprocessing:

The Preprocessing of image contains the operations like RGB to GRAY conversion, Segmentation, Edge detection and Image enhancement etc. The noise occurring in scanning process results in poor recognition of the characters and this problem is overcome by preprocessing the image. The preprocessing comprises normalization and smoothing. The normalization handle the uniform size, slant and rotation of characters and in smoothing some rules are applied to the contents of the image with the help of thinning and filling techniques.

C. Feature Extraction:

The feature extraction is the process of obtaining information about the object or group of objects in order to facilitate classification. This is the important module in the OCR system. The characteristics of the image are called features. It extracts the features of the symbols. In this process the symbols are characterized and unimportant attributes are left out. The feature extraction identifies the features like intersections, open spaces, lines etc. but does not match concrete character patterns. An algorithm is used to implement feature extraction which is concerned with the representation of symbols.

The document applied as input contains several lines of text that needs to be categorized into single character for recognition. The following steps are applied for this purpose: The initial darker pixel is named as the top of the row in the scanned document. The next blank line is detected for the bottom. The area between this top and bottom is the row of characters in the image.

Now each character is identified for the rows. This is obtained by scanning the row vertically from top to bottom. The leftmost pixel of the character is the first darker pixel detected. Now if all the pixels are found to be blank, then this is right of character. The character obtained from the scanned image is normalized to 15 X 15 pixel from any pixel size. This is done by cropping the image using top, left, right, and bottom boundaries. Now the 15 X 15 size cropped image can be converted into array of 15 X 15 binary image using thresholding. Here logic 1 represent black and logic 0 represent white.

D. Pattern Recognition:

The pattern recognition is done by matching the obtained binary format with the existing templates. In order to obtain this, the binary format is divided into 5 tracks and each track is again subdivided into 8 sectors. The matrix is generated corresponding to each track- sector for identifying number of pixels in each region. The obtained track-sector matrix is to be matched with the existing templates [2]. The template which is already existing contain each track-sector intersection value i.e. each track and sector value. The character is identified if all the parameters are matched with the template values. Then each and every font consists unique values in the matrix, this makes it easy to identify each font separately.

E. Post Processing:

The post processing consists of the steps that improve the quality of obtained data like filtering.

III. DESIGN AND IMPLEMENTATION

The implementation of the cheque clearance system is explained with the flow chart shown in figure 3.

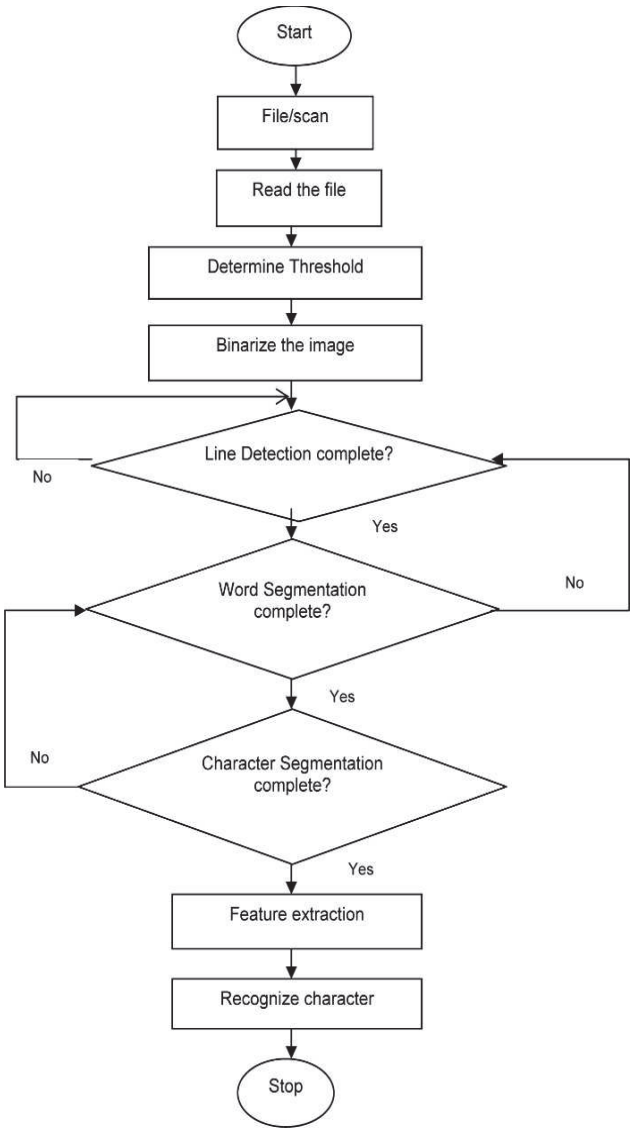

Figure 3: Flow chart for the Cheque Clearance system

Here for the operations to take place, we consider the sample CTS cheque of SBI and fill the necessary details in the cheque and then by using a normal scanner we scanned the cheque and converted it into an image of .jpg format. This process is called Image acquisition in Image processing. Then the image file is read for doing necessary operations on it. The color image is converted from RGB to grayscale, then the image is binarized using thresholding so as to store the image as matrix in digital format. Then the size of the image or matrix is obtained. It is called line or margin detection. Then we determine the necessary fields of the cheque to be extracted and crop it to the new image. This is called feature extraction. The noise obtained from the cropped image is removed by using filtering and segment the cropped image is segmented as individual characters.

We initially have to create the template of characters for both alphabets and numbers for matching with the segmented characters of the cropped image. This is called template formation. Then we have to compare the individual characters with templates created to find the best match. This is called template matching. After the best match is found then we have to store that character. Then we have to calculate cheque number, using those characters as

$$ChequeNum = num(1)\times 10^5 + num(2)\times 10^4 + num(3)\times 10^3 + num(4)\times 10^2 + num(5)\times 10 + num(6)$$

Then we will extract remaining features of the cheque like amount, account number, digital signature and MICR number by using image preprocessing operations followed by optical character recognition algorithm implemented in Matlab.

IV. SIMULATION RESULTS

The scanned copy of State Bank of India cheque with necessary details filled in cheque is taken as input file to extract features as shown in figure 4.

Figure 4: Input file

The binary image obtained after the RGB to gray scale conversion and threshold operation is shown in figure 5.

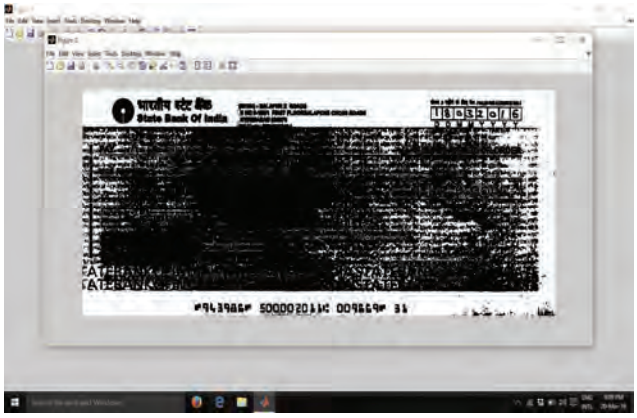

Figure 5: Binary image

Now we go with edge detection to find the areas where key information is located. So we can resize the image and find the number of rows and columns and filter the image for removal of any noise. Now we will crop the cheque number to another matrix. The cropped cheque number stored in another image is filtered for removal of noise. Then we will crop the individual numbers in cheque number for template matching. Templates are either characters or alphabets that are created using a Matlab program as shown in figure 6.

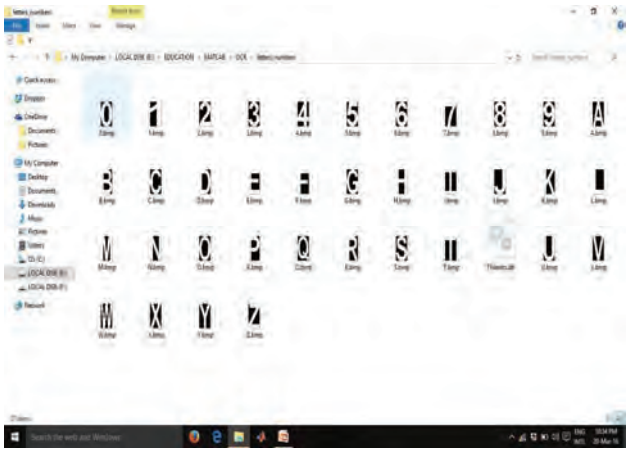

Figure 6: Templates

The extracted individual cheque numbers are then matched with existing templates to find correct match. This is called template matching. Then the cheque number is calculated and displayed from the characters extracted from template matching as shown in figure 7.

Figure 7: Cheque Number Extraction

In a similar fashion the MICR number extracted is shown in figure 8. Similarly the Account number extracted is shown in figure 9.

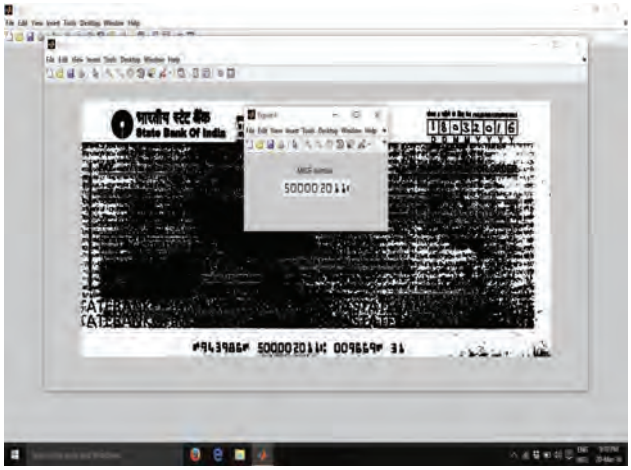

Figure 8: MICR number Extraction

Figure 9: Account number Extraction

Similarly the Amount extracted is shown in figure 10.

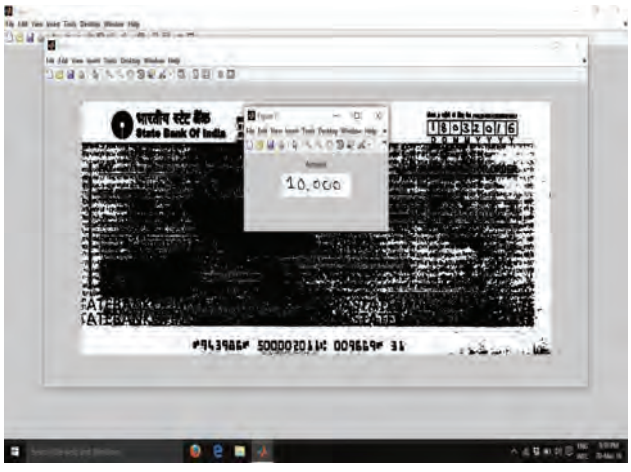

Figure 10: Amount Extraction

Similarly the signature extracted is shown in figure 11.

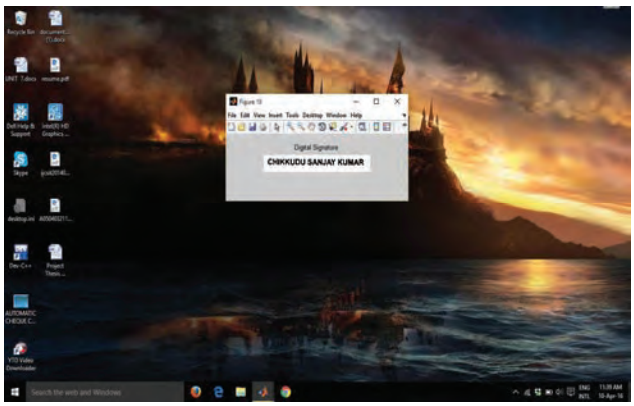

Figure 11: Signature Extraction

V. CONCLUSIONS

In this paper an automatic cheque clearance system is implemented in MATLAB using image processing applications. The different fields in the Cheque truncating System (CTS) compliant cheque like cheque number, MICR number, amount, account number and signature are extracted by using Optical Character Recognition (OCR) technology by image processing concepts which are feature extraction and pattern recognition. Using this one can reduce the human effort, time and money for automatic processing of cheques. The results are obtained for CTS, SBI cheque by extracting cheque number, MICR number, Account number, amount and signature.

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Analysis of Grid connected Doubly Fed Induction Generator based Wind Turbine

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***Abstract*—The most reliable system in the present era to harness the wind power efficiently is grid connected Doubly Fed Induction Generator (DFIG).According to the new grid codes the wind turbines should remain connected to the grid under the conditions of low voltage dips. Semiconductor Magnetic Energy storage system (SMES) coupled to DFIG can improve the voltage stability. The fault analysis of DFIG connected to grid is simulated using the MATLAB simulink and tripping times are recorded for various faults.**

Index Terms— Crow bar circuits, Doubly Fed Induction Generator (DFIG), Low Voltage Ride Through (LVRT), Semiconductor Magnetic Energy Storage (SMES)

I. INTRODUCTION

With the tremendous increase in electrical energy and pollution problems, non conventional energy has become an important energy source. Wind energy has proved to be promising and economical non conventional energy and fast growing renewable energy. Due to its ability to control the pitch angle and produce high amount of power, doubly fed induction generator (DFIG) based wind farms became the first choice of the private wind power generating companies. The terminal voltage and frequency will vary with wind speed and load; whenever induction generator is supplying power to an isolated system , an excitation capacitor is required .Even under the windy conditions also both the voltage and frequency can be controlled smoothly using DFIG

Reduction of mechanical stress on the wind turbine, power quality improvement and increased energy capture are made possible with the DFIG based variable speed wind turbines. Rotor of the doubly fed induction generator is connected to grid through back to back converters, but stator windings of DFIG are directly connected to the electric grid The power electronic converters act as frequency converter and rating of these converters are generally 0.3 times the generated power [1-4].

II. POWER FLOW IN DFIG

The basic block diagram of Doubly Fed Induction Generator Connected to the grid is shown in Fig.1.Here back to back converters with DC link are connected in rotor circuit, the one which is connected to the rotor slip rings is called rotor side converter and the one which is connected to the electric grid is called source side converter or grid converter. The sources of these converters have very low inductance and hence they are voltage sourced converters and the switches that are used in this converter can be turned off by using either voltage or current commutation techniques .The voltage source converter is capable of generating AC voltage from a DC source.

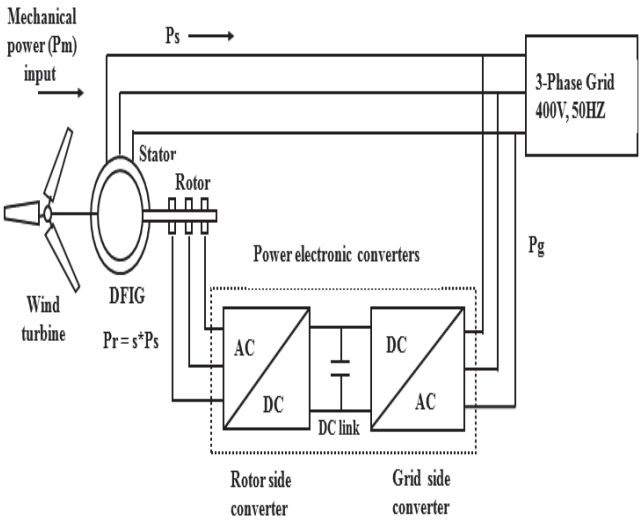

Fig.1.DFIG system with power electronic converters

The two modes of Doubly Fed Induction Generator are namely sub synchronous mode and super synchronous mode. If the speed of the rotor of the induction machine is less than synchronous speed, it operates like induction motor and DFIG is said to be operating in sub synchronous mode and if the rotor of the induction machine is more than synchronous speed, then induction machine is operating like induction generator and DFIG is acting in super synchronous mode. The power in the rotor of a doubly fed induction machine (i.e. of the slip ring type) has three components. These are i) the mechanical power P_m transferred from the rotor to the shaft of the machine; ii) the electromagnetic power or air gap power P_s transferred from the stator windings to the the rotor windings through the air gap iii) the slip power P_r which is conveyed between the rotor winding and any peripheral source or load (e.g. a converter) through the rotor slip-rings. The various components of rotor power during different modes of operation are shown in Fig.2.

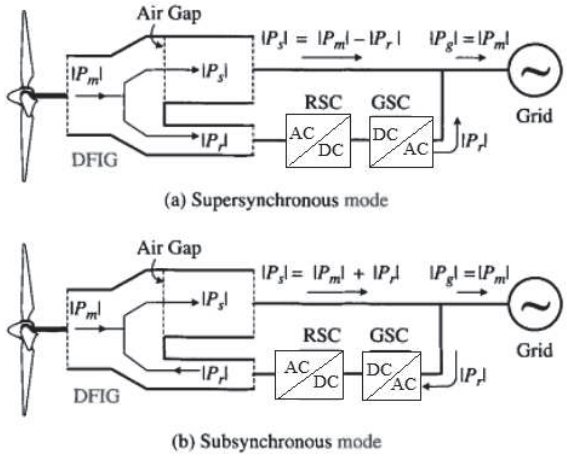

Fig.2.Power flow in DFIG conversion system

Doubly fed induction generator connected to grid can be operated in two modes namely sub-synchronous mode and super synchronous mode .Rotor speed of DFIG is less than the speed of rotating magnetic field in sub synchronous mode. During this mode of operation motoring torque is produced. In order to use the motoring torque rotor circuit of DFIG needs negative power. This can be attained by regulating the voltage that is infused to the rotor circuit. Now the rotor circuit receives the power from the source though source side converter and DC link capacitor.

In super synchronous mode of operation rotor speed of DFIG is more than the speed of rotating magnetic field and slip is less than zero. In order to provide additional generating power to the grid from the charged DC link capacitor, the phase sequence of either rotor currents or rotor voltages must be inverted. Due to the variations in the velocity of wind, the magnitudes of currents in the rotor circuit and hence as a result, rotor voltages also change

III. DFIG WITH SMES

In spite of good performance of the DFIG, there are some problems which are to be addressed when large capacity wind farms with DFIGs are to be linked with the electrical grid. The foremost quandary is the power quality induced due to variations of power. The ability of doubly fed induction generator to control the variation in voltage is pretty low, particularly in windy and turbulent situations. The next quandary is the functioning of DFIG at the time of faults which are occurring in the electric grid. Faults that occurs in the interconnected power system, even very distant from the location of the wind farm, can create a voltage plunge at the common point of coupling of the wind turbine and grid. The plunge in the grid voltage will result in boosting in stator current of the DFIG, as a result over currents are induced in the rotor of DFIG and back to back converters. As the large capacity wind farms with DFIGs are penetrating in to power system network, the ride through competence is almost obligatory and stipulated for DFIG to diminish the undesirable and worst effect on the stability of the power system. One of the preferred solutions to crack the above mentioned problems is the energy storage unit which can handle the transfer of energy caused by variations in power or grid fault [5-9].

A chopper connected across the DC link of a doubly fed induction generator can control the amount of power generated as well as energy storage system, This energy storage system made up of super mantic material, possess highly efficient energy storage, fast response and power controllability The SMES unit is operated to trim down the power quality issues caused by power variations and enhance the under voltage ride through fault capability for the large scale DFIG based wind farms connected to the grid

The circuit diagram employing SMES unit for controlling DC link voltage for a doubly fed induction generator is shown in Fig.3.The excitation system is comprising of back to back converters with DC chopper and super conducting magnet generally made up of niobium titanium(NbTi) or niobium tin(Nb_3Sn). The excitation system in the energy storage unit must possess the properties of good dynamic power response and high energy storage efficiency. So, the superconducting magnet is selected as the energy storage unit of the excitation system, it is set at the DC side of the two converters. The DC chopper is efficiently operated in order to control the power transfer effectively between the super conducting magnet and the rotor of the DFIG or the power grid.

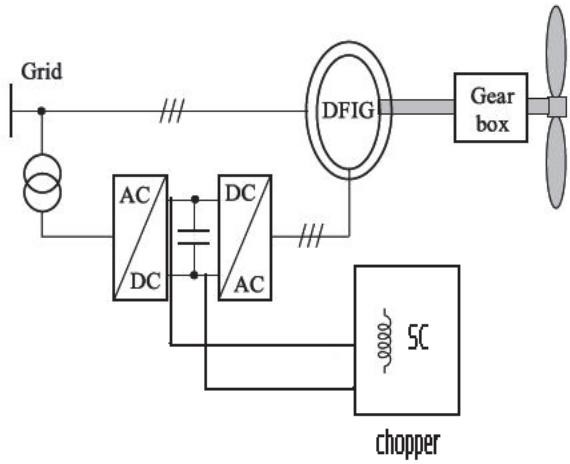

Fig.3.The circuit diagram of DFIG wind power system based on SMES

III. VOLTAGE DIPS AND UNDER VOLTAGE RIDE THROUGH

Involvement of research studies and wind farm developers have confirmed that faults occurring in the electric grid, badly affect the concert of the wind farms. The different types of faults that affect a wind farm are summarized in [10] and are broadly categorised as symmetrical and non-symmetrical faults. Real grid codes specify only about symmetrical faults, because they affect the stability of the electric grid very harmfully. But non-symmetrical faults are further challenging to deal with doubly fed induction generators.

According to new grid code requirements, the large capacity wind farms must stay connected to grid even under conditions of severe voltage dips. If the wind farm is suddenly disconnected, it further contributes to the voltage dip, with terrible consequences. Under the conditions of voltage dips, the stator voltage of DFIG suddenly decreases. Due to this the stator flux cannot track stator voltage. As a result, the stator flux becomes almost stationary. The rotor keeps on rotating and high slip is generated (as synchronous speed of the induction motor is very low).Since the rotor induced voltage is proportional to slip; high voltage is applied across the rotor side converters. Hence a security mechanism is needed to guard the power electronic converter connected to the rotor from the over voltages and over currents caused by the voltage dips.

The standard practice to crack the problem of voltage sags is to connect a crowbar circuit to the rotor of the wind generator. In case of voltage dips, crowbar circuit shorts the rotor of DFIG and the power electronic converter connected to the rotor is safely protected [11]. Even though there are many types of crow bar circuits available, diode bridge and anti-parallel thyristor types are most commonly used Usage of less number of thyristors and easy controllability made the diode bridge crowbar circuit more attractive than anti-parallel thyristor and other crow bar circuits. The crowbar circuit is triggered on, under two different situations. Firstly when DC link capacitor voltage reaches saturation, or when current in the rotor circuit exceeds the pre determined value. Crow bar is activated, since there is no control on the turning off of thyristors. According to the new grid codes , the wind farms should be connected to the grid during the voltage dip. Grid codes of the different countries of the world need not be similar. Some of the grid codes (Grid code of E.on, a major utility company in Germany) are very particular about the reactive power contribution of the wind farms under voltage dip conditions and hence to maintain power factor in the desirable range. The Rotor side crow bar circuit is shown in Fig.4.

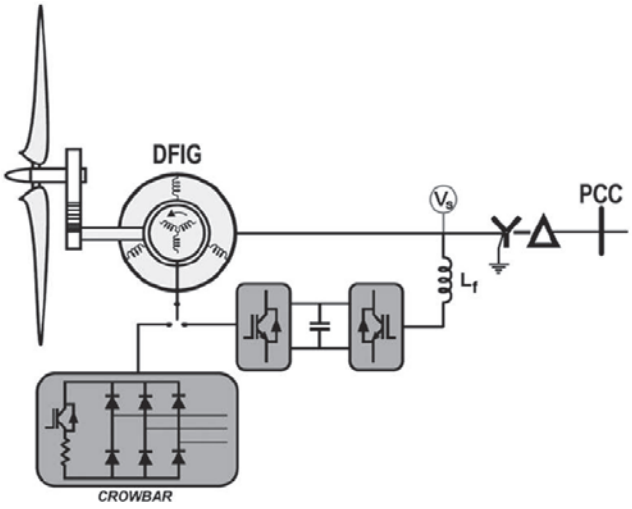

Fig.4 Classical rotor-side crowbar

There are several draw backs of rotor side crowbar. Major drawback is, DFIG loses its controllability once crowbar circuit is triggered. In the above mentioned situation DFIG absorbs huge amount of reactive power from the grid which makes further decrease in the grid voltage. In order to overcome the above drawback, Stator side crowbar circuit was proposed in [12-14] as shown in Fig.5

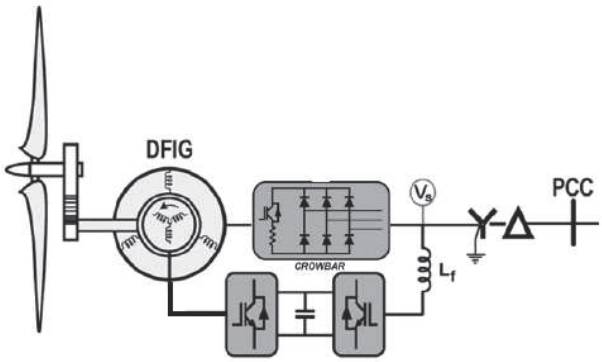

Fig.5. Stator side crowbar circuit

The limitation of stator side crowbar circuit is, its conduction losses are high because the bi-directional switches are in on condition during normal operation. Care should be taken while designing the power electronics so as to minimise the losses.

Another approach for low voltage ride through problem is using Energy Storage System (ESS) .In this system an effective energy storage system placed in between rotor side converter and stator side converter across the dc link capacitor voltage is shown in the Fig.6. Energy storage system simply consists of two bi-directional switches connected in series and ESS connected across one of the switch. ESS based methods have ability to control the doubly fed induction generator during the fault too. Necessity of additional energy storage systems leads to the additional cost and increases system complexity [15-17].

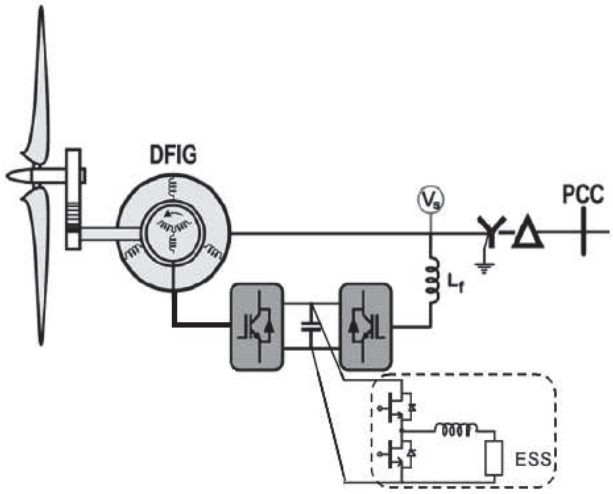

Fig.6 DFIG-Based wind turbine equipped with ESS

Connecting a parallel grid side rectifier (PGSR) with series grid side converter (SGSC) is an alternative

approach to solve the under voltage ride through problems as shown in Fig.7. In this, circuit arrangement generator side converter recuperates the slip into DC link as in conventional doubly fed induction generator. The major function of series connected grid side converter is to inject the DC link power into the electric grid. Using this concept, the amount of power flow can be controlled over typical range above and below synchronous speed. But DFIG suffers at sub synchronous speeds [18].

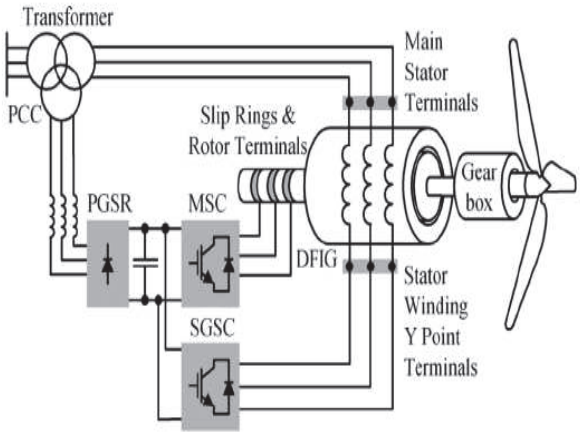

Fig.7 DFIG based wind turbine with PGSR and SGSC

IV. Simulation And Results

A DFIG wind farm comprising of 6 units, each of 1.5 MW capacity (total of 9MW) is simulated .The wind farm exports power to the electric grid of 120kV by a 30km transmission line which is maintained at 25kV. A 2.3kV, 2KVA plant consisting of inductive load and a 200kW unity power factor load is connected to the same feeder at 25 kV bus. MATLAB SIMULINK diagram of wind farm with capacity of 9MW joined to 120kV grid is shown in Fig.8

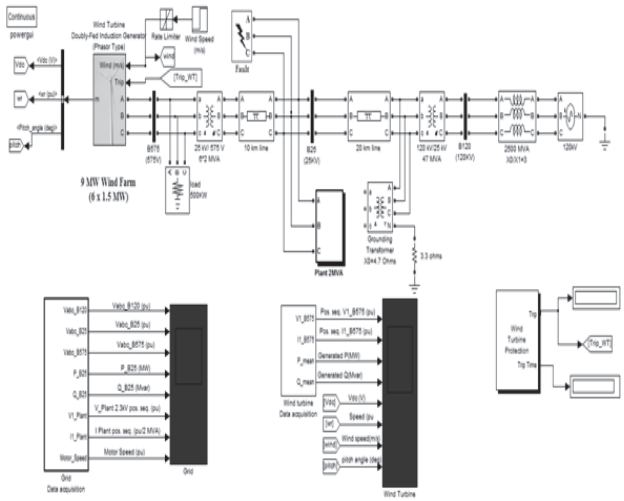

Fig.8 Simulation diagram of a 9MW wind farm connected to 120kV grid

A. *Simulation of voltage sag on 120kV bus system*

Voltage sag resulting from a remote fault is simulated and its effect is observed. A 0.15 pu voltage drop lasting 0.5sec is programmed to occur at 5000ms Control mode of the wind farm is in VAR regulation with zero active power reference and velocity of wind is set at 8 m/s. We observe that wind farm produces 1.87MW and at t=5000ms the voltage drops 0.9 pu and at 5.22sec. Now the plant trips because an under voltage is lasting for more than 200ms has been detected. The plant current falls to zero. The wind farm active power P and plant current are shown in Fig.9

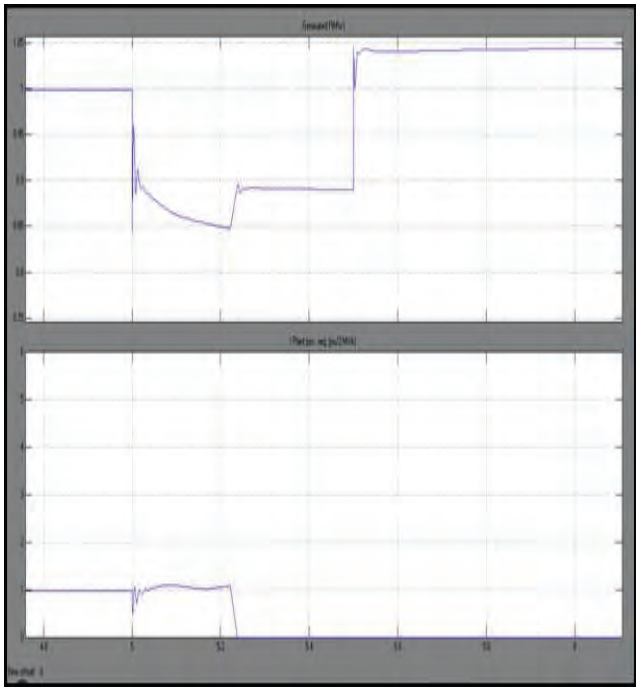

Fig.9. Wind farm power and plant current for a voltage sag.

B. *Simulation of fault on 25kV system*

An L-G fault is programmed to occur at 25kV line at B25 bus. Fault is programmed to occur at t=5Sec.During the voltage regulation mode of turbine, the positive sequence voltage at the terminals of wind turbine drops to nearly 80% during the fault, which is above threshold value(75%) and now wind farm stays in operation even under fault conditions. Voltage and power of the wind farm are shown in Fig.10.

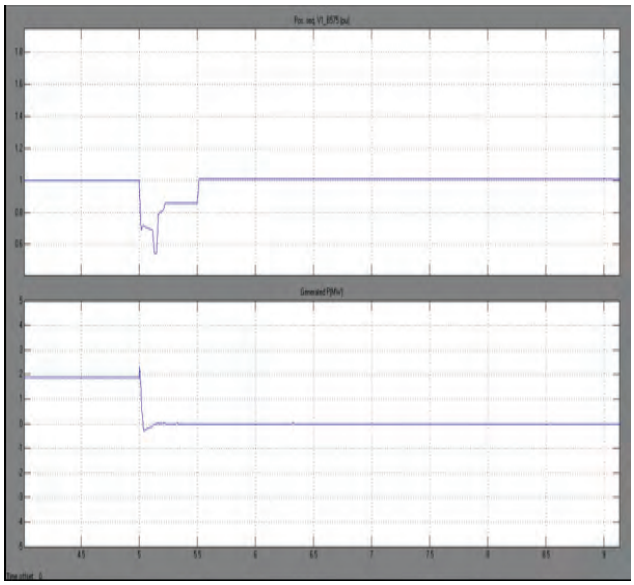

Fig.10.wind farm voltage and power for L-G fault in voltage regulation mode

C. *Simulation of fault on 25kV system with VAR regulation*

Different types of faults both symmetrical and asymmetrical faults are simulated on 25kV bus with wind turbine control parameters in VAR regulation mode. It is found that when the voltage of the wind farm drops to 70% of base value, the under voltage protection trips the wind farm. TABLE I shows the tripping times of the wind farm for different types of faults.

TABLE I.

TRIP TIME OF WINDTURBINE FOR DIFFERENT FAULTS

Type of Fault	Trip time in ms
L-G	115
LL	110
LL-G	108
LLL	10
LLL-G	10

D. *Simulation of L-G fault on 25kV system for various values of ground resistance*

The system is simulated for different values of ground resistance under L-G fault on 25 kV grid and trip times of the wind turbine coupled to DFIG connected to grid are calculated. It is observed that as the ground resistance is increases the fault time is decreased. TABLE II shows the tripping times for various values of ground resistance for single line to ground fault on the grid.

TABLE II.

TRIP TIME OF WINDTURBINE FOR DIFFERENT VALUES OF GROUND RESISTANCE

Ground resistance in mΩ	Trip type in ms
0.01	10
1	9
1000	5

E. *Simulation of L-G fault on 25kV system for various values of Transmission line lengths*

A 9MW Doubly fed induction generator connected to 25kV grid is simulated for L-G fault on grid for different values of transmission line lengths and is found that trip time increases as the transmission line length increases indicating that DFIG trips at faster rate for the faults nearer to the DFIG. TABLE III shows tripping times of wind turbine for different values of transmission line lengths for L-G fault on grid.

TABLE III.

TRIP TIME OF WINDTURBINE FOR DIFFERENT VALUES OF TRANSMISSION LINE LENGTHS

Transmission line length in kM	Trip type in ms
6	112
8	113
10	115

V. CONCLUSIONS

In this paper, basic operation of the DFIG and power flow in the DFIG are discussed. The performance of DFIG along with Superconducting magnetic energy storage system is studied. Effect of voltage sags and low voltage ride through capability of DFIG and different configurations of crow bar circuits are also discussed. A Matlab simulink model of DFIG connected to the grid is simulated for different types of faults and the trip times of the wind turbine are recorded and found that as the intensity of the fault increases the trip time of the wind farm decreases.

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Hybrid Diesel-Electric Propulsion Systems

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***Abstract*—Recent demands for train traction systems require that they have improved energy efficiency. Issues such as global warming and the depletion of energy resources began to attract attention in society. This system provides regenerative braking which has not been previously possible on conventional diesel-powered trains and enables increased energy savings via regenerated energy. It can be used with urban or sub-urban services with two to three coaches, for shunting purpose or mainline service.**

***Index Terms*—Hybrid, Diesel-Electric, VVVF, IGBT Inverter, Battery**

I. INTRODUCTION

Most systems use a series-hybrid configuration that first converts the engine output into electrical power and uses only motors for propulsion. The AC output generated by the engine-generator set is converted to DC. A Variable Voltage Variable Frequency(VVVF) Inverter drives the Induction motors. Storage batteries are connected to the DC link [1]. The charging and discharging of the storage batteries is controlled using output adjustment of the Converter and Inverter.

II. CURRENT CONFIGURATIONS

A. Hitachi series hybrid diesel-electric train

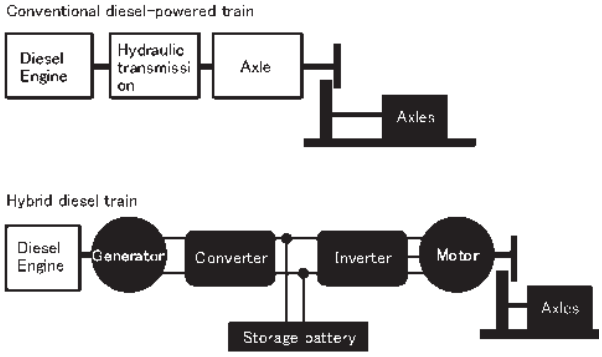

Fig. 1.1: Conventional and Hybrid locomotive configurations.

As shown in Fig 1.1, a conventional diesel powered train, the diesel engine drives axles through a hydraulic transmission. This transmission is sometimes replaced by a generator -motor set, where the motor drives the axles. Control is achieved by placing a suitable power modulator in the electrical connection between the generator and motor.

In a Hybrid diesel train, the diesel engine drives the AC generator. The output of the AC generator is rectified to produce a DC link. This DC link provides the input to a VVVF inverter, which drives the Induction motors. Storage batteries are connected to the DC link. Charging and discharging of storage batteries are controlled by the output adjustment of converter and inverter. The diesel engine-generator set can run at a fixed speed irrespective of the train speed.

B. System Control

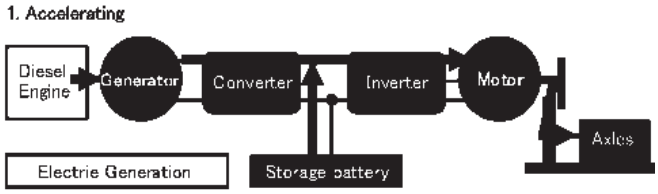

Fig. 1.2: Power flow during acceleration.

As shown in Fig 1.2, the train starts by using the power from the batteries. In the mid-speed range, additional power required is supplied by the engine-generator set.

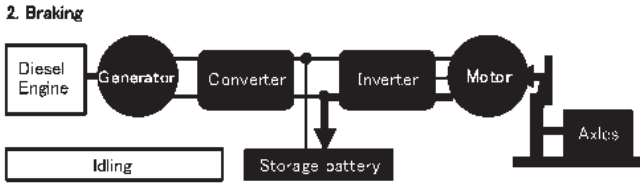

Fig. 1.3: Power flow during braking.

As shown in Fig 1.3, the engine is shut down and the regenerated power from the motor, which is now working as a generator is used to charge the batteries.

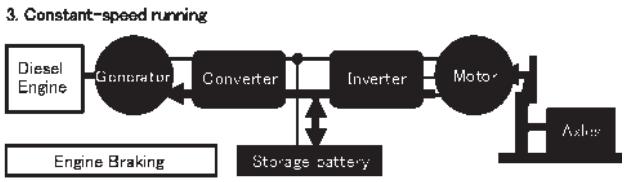

Fig. 1.4: Power flow during constant speed running

Power from both sources is used during constant speed running. To brake at constant speed, engine braking is used. The engine slows down the system and prevents overcharging of the batteries on continuous down-hill gradients.

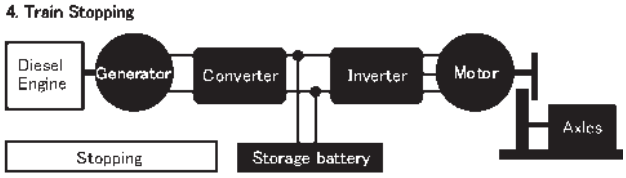

Fig.1.5: Diesel engine is shut down when the locomotive is stationary.

As shown in Fig. 1.5, when the train is stationary, engine is shut-down to prevent noise in stations and it also reduces fuel consumption.

Battery Management

Stored energy must be maximum in the battery during start-up for achieving high acceleration. Similarly, stored energy should be minimum during start of deceleration for absorbing more regenerated energy. The energy management system ensures that optimum amount of energy is stored in the battery to suit the speed range. The output of the generator is adjusted such that the sum of train kinetic energy and stored energy in the battery is always constant [2].

Converter control at constant power

To manage the energy balance in the DC link, the converter is controlled at constant power. As the battery is connected in the DC link, converter control at constant voltage is not possible. The DC link voltage varies with the amount of stored energy in the battery. The converter control at constant power allows optimum charge and discharge control of the battery.

Engine Brake Control

During braking at constant speed, the traction motors generate the braking power. This power flows into the DC link and is distributed between the battery and the converter. The converter is now made to work as an inverter and it drives the alternator as a motor. The engine now acts as a load on the alternator to control the speed. This method provides stable and constant speed under any running conditions.

C. Toshiba Shunting series hybrid Locomotive

The shunting hybrid locomotive shown in Figures 1 and 2 uses large capacity high performance batteries. The locomotive can haul a load of 1300 Tons using the power source from the batteries alone. PMSM is used as traction motor. During normal operation, power flows from engine-generator set and battery to traction motors through the inverter. During braking operation, the regenerated power is used to charge the batteries. The system uses lithium – ion batteries. The main battery capacity is high enough to start the locomotive. Modular design has been adopted and each module can be replaced individually. Nitrogen oxides in the emissions were 62% lower and fuel consumption was 36% lower when compared to a conventional diesel-electric locomotive. The diesel engine has a power rating of 270 HP while the generator is rated at 173 KVA. The maximum power output of the locomotive is 500 KW. The locomotive can achieve a top speed of 45 KMPH at full load and a top speed of 110 KMPH at no-load. The system has a modular design. Each module can be replaced with a more recent technology in the future. For example, the diesel engine can be replaced with a fuel-cell and the IGBT based inverter can be replaced with a SiC hybrid inverter. [8].

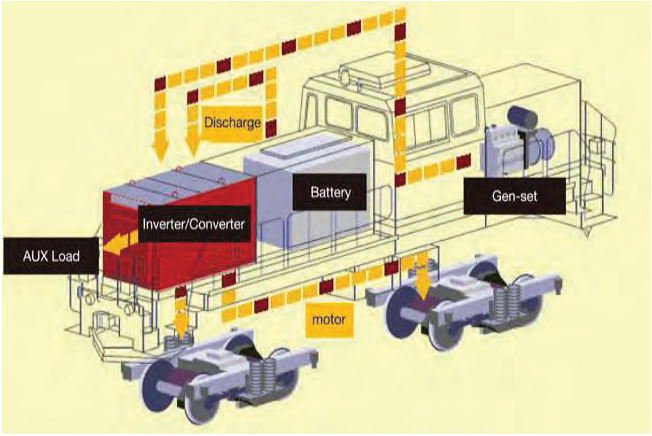

Fig. 2. During acceleration, the control optimizes power flow to the traction motors from both sources or power flows from battery alone.

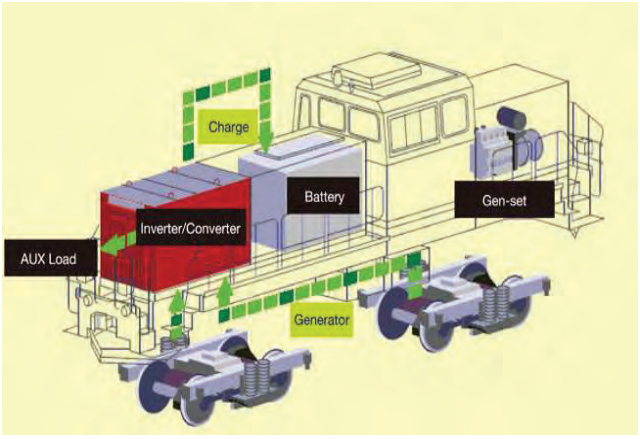

Fig. 3. During deceleration, the power output from the traction motors is used to charge the batteries. The control protects the batteries from over charging or deep discharging.

The locomotive has four inverters connected to four traction motors. Each traction motor is coupled directly to the axle. If a particular inverter or traction motor fails, the locomotive can continue operation with reduced capacity. Redundancy is provided in the battery module. If a battery fails, the locomotive can continue its operation with the defective battery isolated. The converter uses PWM control. The system is controlled by the control unit with a CPU. This control unit controls the converter and inverter for various functions such as acceleration, deceleration and braking. Due to the modular design, maintenance of the locomotive is also simple. If batteries of higher power density are available in the future, they can be used with this locomotive to increase its output power. It also offers the advantages of reduced life-cycle cost and reduced fuel cost. The Permanent Magnet Synchronous Motor (PMSM) used for traction also offers high efficiency [3].

C. Railpower Shunting Hybrid Locomotive

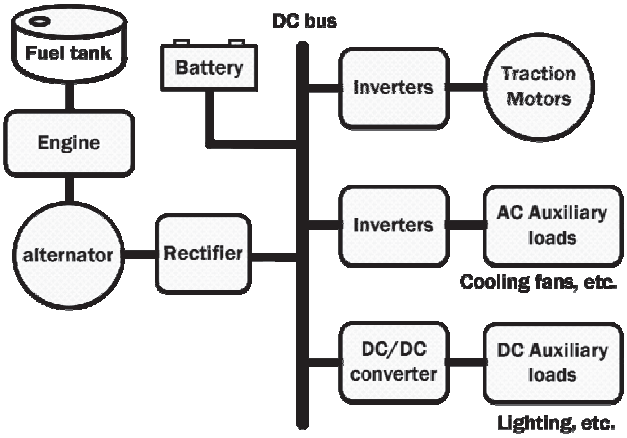

Fig.4 Block diagram of Railpower series hybrid diesel electric locomotive

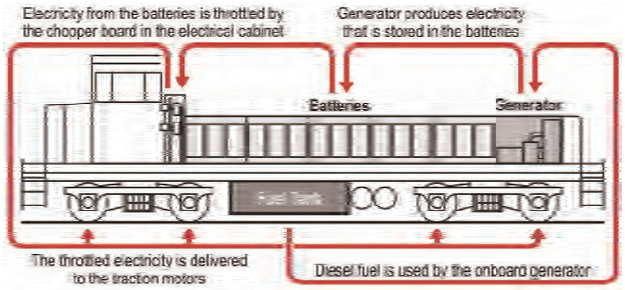

Fig.5 System operation in Railpower hybrid diesel electric locomotive.

As seen in the figure above, the engine -generator set is used only to charge the batteries. The output power from the batteries is supplied to traction motors. This method helps in reducing the idle running time of the diesel engine and contributes to 40-70% savings in fuel costs and up to 85% reduction in emissions. The prototype's diesel engine had a power output of 216 KW and a total output of the locomotive was 1490 KW.

D. Application of parallel hybrid technology in main line diesel-electric locomotives

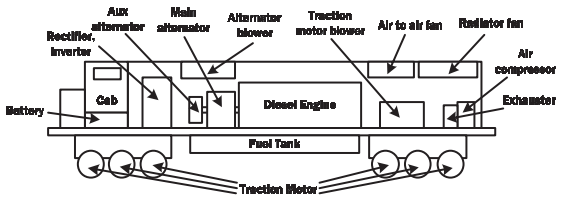

Fig.6 Block diagram of main line diesel-electric locomotive.

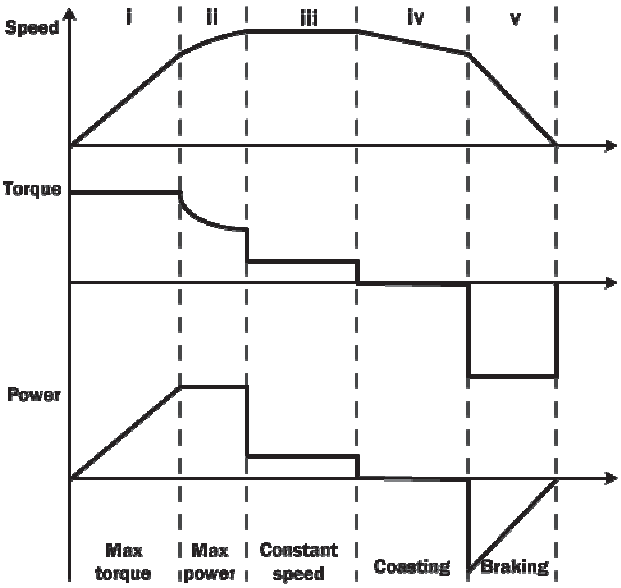

Fig.7 Operating profile of a mainline locomotive.

The basic block diagram and operating profile of a mainline diesel-electric locomotive are shown in figure 5 and figure 6 respectively. Mainline locomotives are used for inter-city service and haul passenger or freight trains. The torque demand is severe during starting and decreases as speed decreases. Torque and power become negative during braking operation. Typical power rating of a mainline diesel-electric locomotive is 4500 HP.

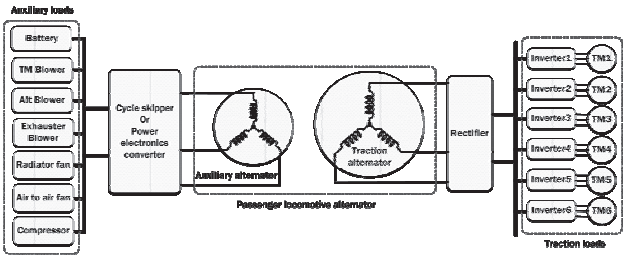

Fig.8 Electrical connection of alternators in a diesel-electric locomotive with traction motors and auxiliary loads.

The diesel engine drives two alternators connected to the same shaft. The main alternaor supplies power to the six traction motors through the converter-inverter. The second alternator is of lower power rating than the main alternator and supplies auxiliary loads [5]. Each traction motor has a separate inverter. In large locomotives, the power regenerated during braking is stored in batteries. These batteries are Sodium metal Chloride (Lead free) rechargeable batteries. When fully charged, the locomotive can run an additional 2000 KM using the battery power alone. Fuel consumption is reduced by 15% and emissions are reduced by 50% compared to a similar diesel-electric locomotive [4].

The locomotive was designed and manufactured by General Electric (GE). It is the only locomotive that meets the most recent emission norms for locomotives in the

United States. The locomotive has a rated output power of 3280 KW [9].

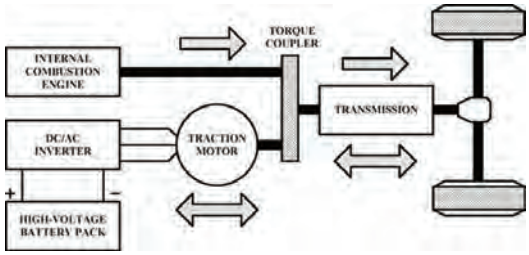

Fig.9 Block diagram of a parallel hybrid system used in mainline diesel-electric hybrid locomotive.

E. Alstom parallel hybrid shunting locomotive

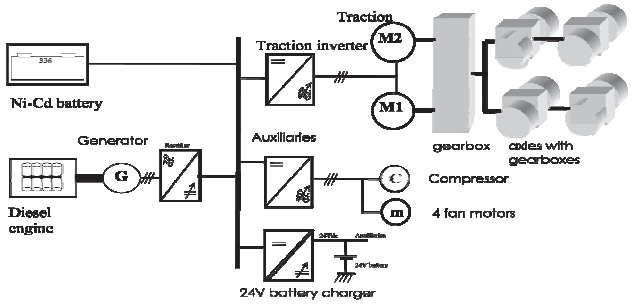

Fig.10 Block diagram of Alstom shunting locomotive using parallel hybrid system.

This locomotive uses Nickel-Cadmium(Ni-Cd) batteries.

The diesel engine-generator set runs at a constant speed irrespective of locomotive speed. The idling time of the engine-generator set is used for charging of the batteries.In normal diesel-electric shunting locomotive, fuel is simply wasted during idling time. Various modes of operation of Alstom locomotive are shown in the figures below [6].

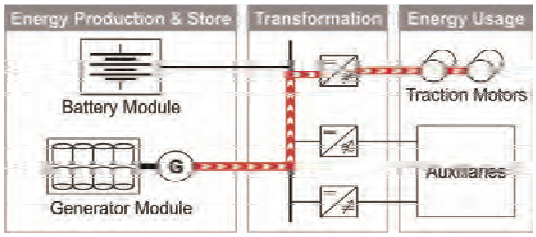

Fig. 10.1 Mode – I: Power flows from diesel engine to traction motors during light load.

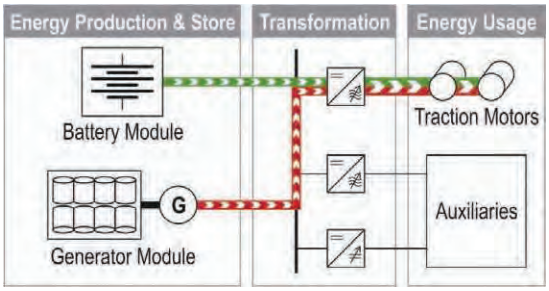

Fig. 10.2 Mode – II: Power flows to traction motors from both sources during heavy load.

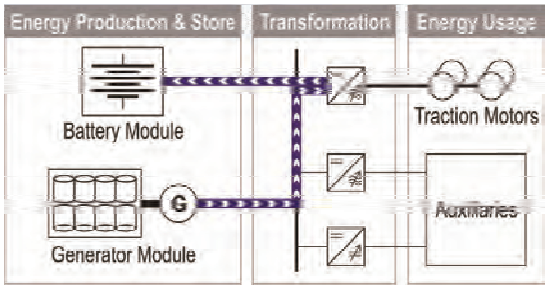

Fig.10.3 Mode – III: Power flows from diesel engine to batteries during idling.

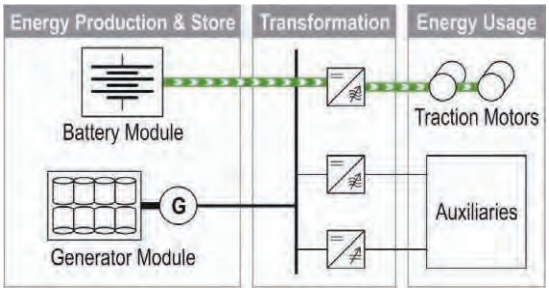

Fig 10.4 Mode – IV: Power flows from traction motors to batteries during braking.

III. SUMMARY

Locomotive	Type	Hybrid system	Diesel engine power	Total power output	Battery type
Hitachi Ki Ha E200	Diesel Multiple Unit (DMU)	Series	330 KW	430KW	Li-ion
Toshiba HD - 300	Shunting	Series	205 KW	500 KW	Li-ion
Railpower GG-20B	Shunting	Series	216 KW	1490 KW	Li-ion
GE Evolution Hybrid	Mainline	Parallel	3280 KW		Sodium metal Chloride
Alstom BR-203H	Shunting	Parallel	200 KW	550 KW	Ni-Cd

IV CONCLUSIONS

At present, hybrid technology is best suited for shunting locomotives. A shunting locomotive travels less distance, starts and stops frequently and has a very high idling time when compared to running time. All of these conditions are suitable for effective charging and discharging of batteries in hybrid system. An outstanding advantage of the hybrid system is the possibility of regenerative braking and effective use of regenerated power. With advances in battery technologies, hybrid technology might find wide spread application even in mainline locomotives.

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LabVIEW based Sliding Mode Control of a pH Neutralization System

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***bstract*— This paper targets at designing a control mechanism using the method of Variable Structure Control [VSC] for a pH neutralization process plant. This VSC involves SLIDING MODE CONTROL (SMC). The prototype pH model involves acidic and alkaline reagent solutions which in proper quantities are mixed into a Continuous Stirred Tank Reactor [CSTR] in proper proportions. The pH of the plant is in turn controlled by the same. The flow rate of acid and alkaline solutions is controlled by the control mechanism. SMC is a type of nonlinear control. The pH neutralization process is a best example of non linear system; hence SMC offers a better solution. SMC suffers a problem called chattering, to overcome this, Dynamic Sliding Mode controller can be implemented. LabVIEW software is used to implement the controller. LabVIEW is the acronym for Laboratory Virtual Instrumentation Workbench. The prototype model is subjected to this programming method and the results are presented. This is a graphical programming technique. The interfacing of the software and the prototype hardware is done using DAQs.**

***Index Terms*-- Variable Structure Control, Sliding Mode Control, Ph Control, LabVIEW**

I. INTRODUCTION

Contaminants such as organic substances, heavy metals, suspended solids and cyanides are present in wastewater from several industries. This poses potential health risks and also its hazardous to public and environment. The techniques used in the convention treatment of wastewater involve precipitation of heavy metals, flocculation, settling and discharge [1]. Apart from addition of chemicals, the treatment involves adjustment of pH also. This makes pH control a highly non linear process [2]. By manipulating an acid and an alkaline stream the pH is monitored and controlled. Several modern treatment processes use both physical and chemical precipitations where neutralization of pH is the prime factor for effective treatment. A pH sensor is used in most processes for the on-line measurement and control. In this paper, LabVIEW software is used to operate and control the system automatically by an online computer. Frequent load changes and severe non linearities make the pH control in a wastewater treatment process very difficult [3]. The primary source of the non-linearity is the S – shaped titration curve. In this paper using VSC, a possible better control of pH in a wastewater treatment process is suggested. To indicate the robustness of VSC few studies have been done in the non linear control area [4].

A. Variable Structure Control [VSC]

SMC is a type of Variable Structure Control (VSC). In control system engineering theory, SMC, is a type of a non linear method which applies a discontinuous signal to the process and in turn alters its dynamics. This in turn forces the system to "slide" on a surface which is equivalent to the systems general behavior [5]. In SMC, the control law governing the system is not a continuous function of time. Still depending on the present position it can switch from one continuous control structure to another continuous control structure in their corresponding state space. Because of the above mentioned characteristic, the SMC is considered as a robust controller which can overcome the problems of non linearity [6]. Several control structures are designed in such a way that the trajectories move to towards nearby regions, thereby resulting in having a trajectory with different control structures. This trajectory will tend to slide along the borders of the control structures. Sliding mode term is used due to this movement of the system, as it slides along these boundaries. The sliding (hyper) surface is the locus consisting of the sliding mode boundaries. So we have a flexibility of having a system with different control structures but with a common trajectory.

Fig. 1 represents the sliding surface of a system with the trajectories. s=0, is the equation representing the sliding surface, also the sliding begins after the trajectories reach the common surface after a finite time. Practically the sliding occurs the control signal incurs high frequency switching and this causes the system to CHATTER in its adjacent control structures [7]. From the figure it can be seen that the system is subjected to chattering phenomenon. Although it experiences chattering asymptotically it reaches origin [8]. This response makes the system act like a linear control system. Though the system is non linear, but when it confines to the surface s=0, it exhibits the idealized (i.e., non-chattering) behavior with a stable origin. An infinite gain is used to force the trajectories to slide along the subspace of the sliding area [9]. Using reduced-order sliding mode, the systems obtains desirable properties such as, allowing the system to slide smoothly along its trajectories until it reaches its desired equilibrium. As the switching involves transfer between two states i.e. ON/OFF, the parameter disturbances does not affect the performance of the controller. This property of this controller makes it more robust.

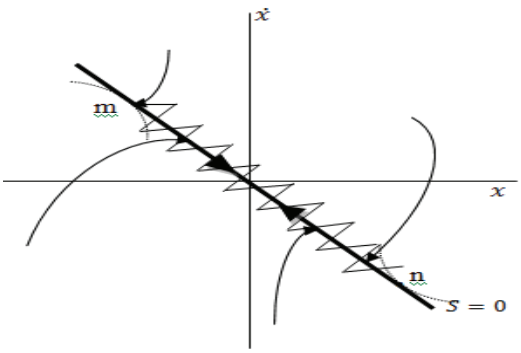

Figure 1. Example of a Sliding Surface

Also the controller need not be precise as it is only the switching between two states and the intermediate points are not considered. As the control law defined is not a continuous function, it makes the sliding mode reach the equilibrium in a *finite* time. This makes the system behave better than asymptotic response. Due to this behavior SMC is suited as an optimal controller for several dynamic systems. One application of SMC is the electric drives control which is operated by using switching power converters. Other applications of SMC include robotics. Specific applications includes, tracking control of unmanned surface vessels with good degree of success in simulated rough seas. Compared to non linear control actions that have moderate control actions more care must be applied to Sliding mode control. Few equipments like actuators incur delays and few other imperfections, which leads the sliding mode control to result in effects such as chattering, energy losses excitation of several un-modeled dynamics and plant damage. Continuous Control Design (CCD) methods are advantageous as they are not as prone to such problems and hence can be made to replicate SMC.

II. THE PH NEUTRALIZATION PROTOTYPE SYSTEM

A. Hardware Details

The prototype pH process system consists of three cylindrical chemical tanks each with a capacity of five litres. Each tank contains a base (NaOH), an acid (HCl) and the test solution whose pH has to be measured and neutralized. The three containers are made of special chemical corrosion resist glass. For proper mixing of the above mentioned three solutions another tank is used. This tank is called mixing tank. To provide uniform mixing the mixing tank contains a stirrer. This stirrer is made of fiber glass. The capacity of the mixing tank is 5 litres. A reservoir tank of capacity ten litres is provided additionally. The complete block diagram of the process is shown in Fig. 2. The stirring action is done by a permanent magnet DC Motor. The ratings of the motor are 12 V DC, torque 1kg-cm, 1500 RPM. For temperature compensation, a Resistance Temperature Detector (RTD) is provided. Polyethylene plastic are used for Piping, manual valves and fittings with sizes ranging from 1/8 to ¼ inches.

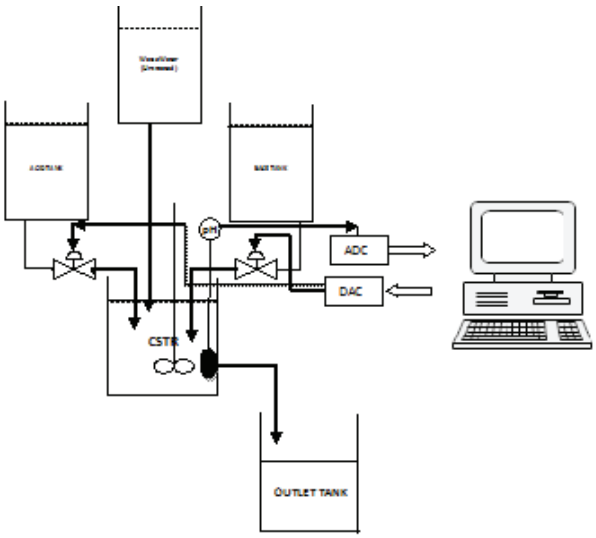

Figure 2: Overall Block Diagram of the pH prototype process

They have the property of chemical corrosion resistance. Pneumatic pressure transfer is done via Nylon tubing. Glass electrode is the type of pH measuring sensor. For regulating the acid and alkaline flow, two Equal Percentage type control valves with two way and normally closed (NC) type are used. The pressure signal 3-15 psi is used as an input to the valves. Both have a body of ½ inch and with a trim of ¼ inch. Teflon is used for acid valve so as to prevent corrosion. The outputs ranging from 3 to 15 psi are provided by two current to pressure converters. LabVIEW software is used to run the process.

B. Experimental Procedure

The setup is cleaned properly before beginning the process so as to remove any contaminated material. The pH electrode sensor is cleaned and calibrated using standard buffer solutions. Using online computer, the experimental runs are achieved. The acid and base reagents are filled in their respective tanks. The interface between the computer and the process setup are verified. Power supply is switched ON only after verifying the power supply to other parts of the process. Using the LabVIEW software the setpoint i.e. the required pH in the tank is set and the SMC control also has to be selected. The process variable i.e. pH of the solution in the mixing tank is sent to the computer through the NI-DAQ input module. This information is sent in the form of the standard current signal of the range 4-20mA. The set point is compared with the pH of the solution of the mixing tank and an error signal is generated. This error signal is manipulated accordingly and a control output is generated. Using the NI-DAQ output module, the controller output is given to the current to pressure (I/P) converter. The input signal is a 4-20 mA varying current signal. An output pressure is generated for a corresponding input current in the current-to pressure converter. The pressure converted is in the range of 3-15 psi. The positioner of the acid and alkaline valves is regulated by this converted pressure. The valves

of both acid and alkaline tanks opens or closes proportionally, thereby giving the necessary quantity of the reagents to regulate the pH of the solutions in the mixing tank. The response can be viewed in graphical format on the computer.

III. CONTROLLER

Process control is an engineering stream that deals with algorithms, architectures and mechanisms for maintaining the response of a process within a specified range. Several controllers are used in process control industries to enable mass production from continuously operated processes such as power plants, oil refining industries, chemicals process industries, paper manufacturing industries and many others.

Sliding Mode Controller

The Sliding Mode Control (SMC) is a non linear control technique, which is a type of VSC. SMC exhibits high insensitivity to parameter variations and disturbances. The Sliding Mode Controller has two parts (i) a sliding surface which is stable and (ii) a corresponding control law which forces the states of the system to reach the selected surface in finite time. Sliding Mode Control is a nonlinear control method. By application of a discontinuous control signal the dynamics of the non linear system gets altered. This control signal forces the states of the system to "slide" along the cross-section of the control structures associated with that system. When subjected to actuators the main problems that are faced by controllers are the imperfections, this in turns leads to chattering, plant damage, energy loss etc. The control action in this process is an action of switching between two states. So the parameters are not affected by external variations or disturbances. The design of SMC is done by first defining the sliding surface. Equation (1) given below is representation of the Sliding Surface

$$S = \delta_s (p_1 - X) \tag{1}$$

where δ_s is a positive scalar.

δ_s represents the slope of the sliding surface .

X is the setpoint and p_1 is the pH obtained from the process.

The corresponding control law which forces the system to the sliding surface is given by

$$u = \frac{1}{\alpha_s}.C\left[\alpha_s.a\sqrt{z_1} - W_s \operatorname{sgn}(S_s)\right] \tag{2}$$

A chattering response is obtained at the output. This occurs due to the shift in the state trajectories due to the discontinuous control law. To minimize this effect a Dynamic Sliding Mode Control is applied. This decreases the chattering and limits it, thereby giving a smooth output.

IV. INTERFACING WITH THE PROCESS PLANT

In this process, pH and flow sensors are coupled, apart from the tanks, with a control and monitoring unit. As pH is sensitive to temperature compensation system is provided to overcome effects of temperature changes. The reactor is made to operate at atmospheric pressure and temperature. The speed of the stirrer is around 1000 rpm. Pumps are provided with the inlet streams, so as to feed the reactor with corresponding solution. The acid stream used in this process is 0.1 M HCl and the base stream used is 0.1 M NaOH. The mixing tank with the stirrer acts as a Continuous Stirred Tank Reactor [CSTR]. To achieve the desired pH, the acidic and the alkaline streams are manipulated. LabVIEW software is used to design the SMC controllers. The data is primarily transmitted to the Virtual Instrument and the VI executes the program and correspondingly the amount of acid and/or base to be added is computed. This in turn is sent as a pressure signal to open or close the control valves of the acid and base stream. The experimental Setup of the process is shown in Fig. 3. The figure shows two tanks on either ends which contains Acidic and Alkaline solutions. The solution whose pH has to be regulated is seen at the centre. Also seen is the Continuous Stirred Tank Reactor [CSTR] which regulates the pH of the solution by mixing the acidic and alkaline solutions in proper proportions. Both the CSTR and the reservoir are placed below the process.

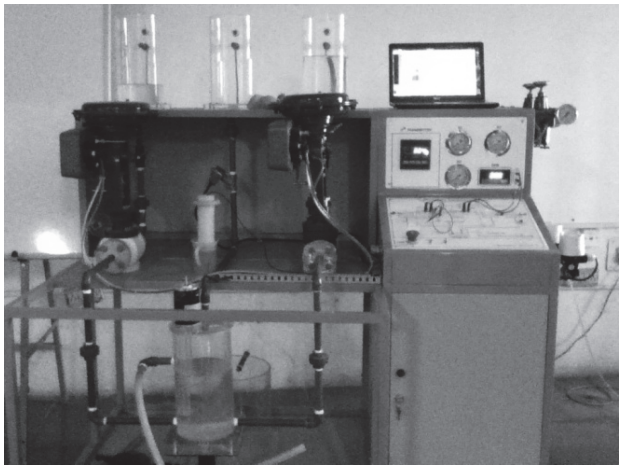

Figure 3: Prototype Experimental Setup of the pH process

V. VIRTUAL INSTRUMENT

The virtual instruments simulating the various control actions are shown. The Front Panel of the whole pH process is shown in figure 4. The controllable features of the system are indicated in it. The ability to change the pH is incorporated. The front panel is programmed in such a way that the user can use the controls on the screen in an easier and user friendly way. The front panel consists of dials, knobs, graduated tanks and graphical display.

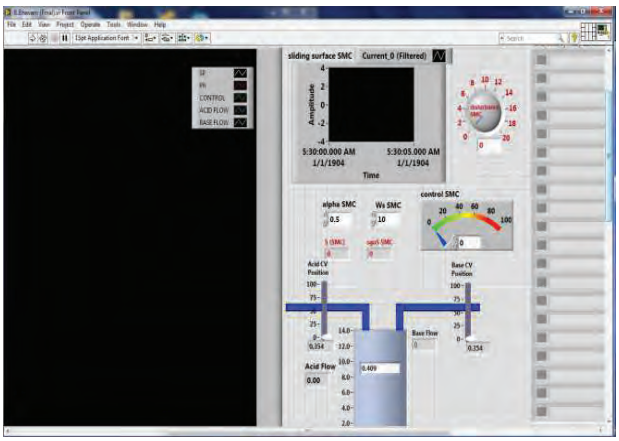

Figure 4: Front Panel of the process

VI. RESULTS

Initially the plant is cleaned to remove any contaminations or residues. The pH electrode sensor is cleaned and calibrated using buffer solutions. Each tank is filled with the respective solutions. Hydrochloric acid in the acid tank and Sodium hydroxide in the alkaline tank. The interface between the prototype process and computer is verified. The required setpoint of pH is selected using LabVIEW software. The responses are observed in both in the virtual tank and also in graphical method. A tabular format of values is obtained by importing the values to Microsoft excel at every instant. The desired pH set point is 13 which have to be maintained in the mixing tank. On application of the Sliding Mode Controller, the following responses are achieved.

Sliding Mode Controller

The pH setpoint level was set at 13.After 30 seconds the output reached the setpoint. The peak overshoot of the response was observed around ±0.2 pH. Figure 5 shows the response of the system on the application of SMC.

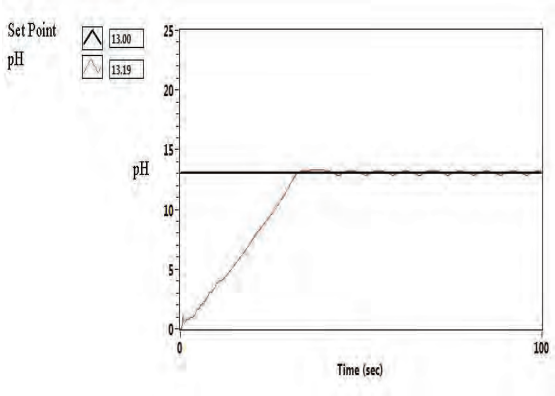

Figure 5: Graph showing response of pH due to SMC

The figure 6 shows the flow rate of acidic and alkaline solution into the tank. It is seen that a lot of chattering is observed. To minimize this effect a Dynamic Sliding mode controller can be incorporated.

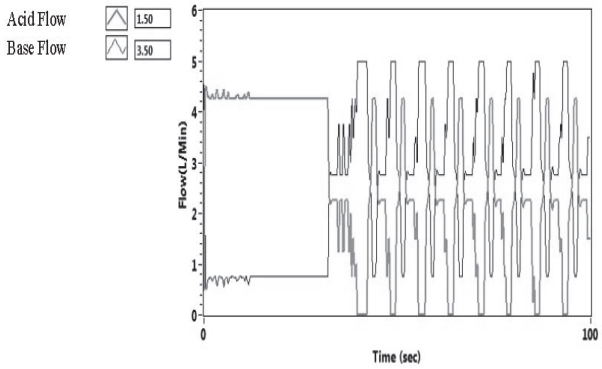

Figure 6: Graph showing the acid and base flows in the tank

VII. CONCLUSIONS

A few researches have been earlier done in this neutralization process. As LabVIEW software is used the results are more user friendly. This paper presents sliding mode control for a pH neutralization prototype process. Physico-chemical principles and fundamental laws are used to achieve process modeling of the prototype process. A mathematical modeling process is incorporated. To estimate the manipulating variables which were unknown earlier, several practical tests are carried out on the actual system. The robustness of the system was increased using the sliding mode controller. Also real time changes were incorporated satisfactorily. The chattering features of the output can be minimized by incorporating a Dynamic mode controller.

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SCADA Based Automatic Direct Reduction of Iron Process using Allen-Bradley Programmable Logic Controllers

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Abstract— **In this paper, we propose an SCADA Based Automatic Direct Reduction of Iron (DRI) Process Using Allen-Bradley Programmable Logic Controllers. SCADA stands for Supervisory Control and Data Acquisition system. The main objective of the project is to get the high grade (high quality) of Sponge Iron. Main quality of the product depends of the temperature of the different junctions of the rotary KILN .Initially, measures the temperatures of the junctions of KILN and fed as inputs to the PLC which in turn sent to PC through RS-232 for necessary processing. A PLC program is developed based on the signals received from the PLC analog input module, process the signals and send the output signals to the PLC output modules, which is programmed to control the fuel conveyor and shell air fan by using PLC-PID controller functions. Here controller parameters can be determined by PID-tuning methods.PLC program can be implemented by considering Rotary KILN direct reduction of iron process.**

The SCADA screens are developed on PC regarding process going in rotary KILN using RS-VIEW SCADA software. The Allen Bradley micrologix 1200 PLC have to be linked up with the supporting SCADA RS-VIEW by giving necessary tag names. With the help of SCADA, simulation of the physical equipment is also developed to monitor the quantities to be measured and status of the in the plant from field point.

Index Terms: **DRI process, Analog I/O Modules, Rotary KILN, PLC and SCADA.**

I. INTRODUCTION

DRI process: Large amount of sponge iron is produced in INDIA only and no. of sources are available in INDIA to get raw material iron ore and we are exporting raw material iron to China also.

Direct reduction of iron is the process of making the steel or iron product .Initially product can be produced by Direct reduction of iron process, This is also called as sponge iron .Initially this can be processed in another way, which is called as pig iron[1]. In this process iron ore can be reduced into lumps and pellets by using reducing gases. This gas can be produced from fuels like coal or gas. Total reduction process is going into the KILN. It is also called as reactor or furnace or rotary KILN. In this process hydrogen and carbon monoxide are the major gases of reducing gas. Here raw material iron ore is fed to KILN along with the coal and dolomite. Dolomite reduces the absorption of sulfur from the coal while reduction process is going.

In this process mainly have seven junctions; each junction takes different chemical reactions in order to produce desired grad of iron .Basically, we have to provide oxygen to produce satisfactory combustion process in the rotary KILN. It takes these chemical reactions b/w 750^0c and 1100^0c temperature levels .Sponge iron plants give good grade of iron products. These plants were established throughout the world. In this Paper rotary KILN junction temperatures can be controlled by adjusting the speed of conveyor belt. Once the speed is controlled then the flow of fuel will be controlled, once the flow of fuel is controlled then the temperature will be controlled and then reduction of iron will be controlled [1]. Here quality of product mainly depends on temperature of gas or breath and the chamber pressure; these parameters can be automated by using PLC and SCADA system.

II. BLOCK DIAGRAM OF THE APPLICATION

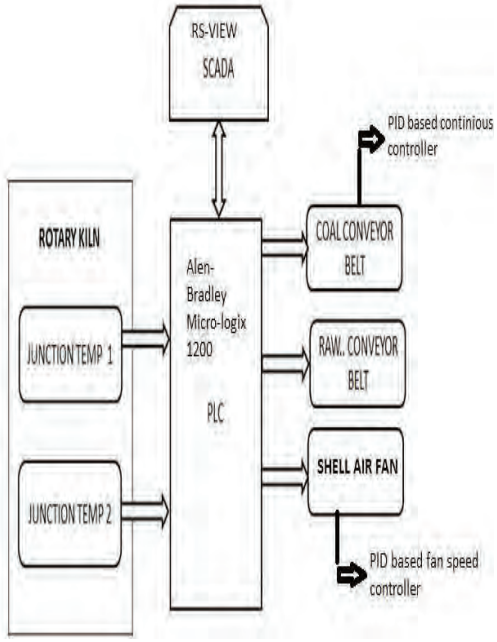

Fig 1.Block diagram

The block diagram Fig.1describes the interfacing of hardware and software i.e., interfacing of input and output field devices with programmable logic controllers. Eight

input field devices are interfaced with the PLC input output modules. In this project eight digital input terminals, two analog input terminals, one digital output terminal and two analog output terminals are used. Eight digital input terminals are used to interface eight starts and stop buttons for on and off of coal conveyor belt, total system on and off switches and Raw material Iron ore on and off switches [2]. These switches are named as sw1, sw2, sw3, sw4, sw5, sw6, sw7 and sw8.Before going to make the connection of field devices ,power supply should be provided to input and output modules of PLC, different PLC's requires different power supply rating, this PLC requires 24 VDC power supply. This will be provided externally (or) some PLC's have in built power supply unit. Depending on the type of application the switches have to be selected like push buttons (or) limit switches (or) toggle switches.

PLC analog modules are required to interface analog measuring devices like thermocouples. In this project we are using K-type thermocouples, which measures temperature from "-200 c to 1300 c" and produces m volts range of signals [3]. These sensors are interfaced to PLC analog input thermals. In this project we are using two thermocouples to measure the temperature at two different junctions of Rotary KILN but to make interface of thermocouples, which requires signal conditioning circuits to meet the desired specifications of PLC analog input modules. This modules has inbuilt analog to digital converters. So no need to use external ADC devices.

Three output module terminals are required to interface output field devices. These devices are named as Dcm1, Dcm2 and Dcm3 [3]. One output terminal is digital terminals and two more terminals are analog output terminals. Here these motors can't be interfaced directly to the output to the terminals of PLC, which requires isolation (or) drivers circuit like Relays, switches…..etc. mostly analog modules requires power amplifier circuits, which are designed with the power electronics devices. Like SCR, thyristers devices [6]. If the DC motor range is 12V then the circuit will be designed with electronic devices like diodes, transistors, resistors...etc.

Here output devices will be controlled by the PLC solid state equipment. The speed of the conveyor motor depends on the junction temperatures at the KILN. We need to develop the program for PID controller by using PLC –PID functions in order to get desired control action on conveyor motor [4]. If the temperature of the Rotary KILN exceeds the tolerance value (or) desired value then PID controller sends the control signals to the fuel conveyor motor unit to get the desired temperature at the junctions of KILN. Here the quality of the product depends on the maintenance of junction temperatures.

III. I/O DEVICES, KILN AND SPECIFICATIONS

The devices which are interfaced from the field of industry to PLC input and output terminals are called as field devices which are like switches, sensors, motors and lights .The following devices are interfaced with PLC I/O terminals.

Rotary-KILN: A Rotary-kiln is temperature processing unit is shown below Fig.2. Rotary KILN is also used in cement and pharmacy industries for combustion process, which is driven by PLC through variable frequency drivers. This is acting as a furnace, three raw materials are fed to KILN, and these are iron ore, coal and dolomite. KILN is designed with protected seven layers so temperature cannot be radiated into the environment. Oxygen gas is supplied to KILN to get combustion process. Which is operated for 600^0c to 1200^0c while the KILN is rotating then slowly raw material moves down towards the lower end while raw material is fed into the upper end of rotary KILN. Exhausted pressure is released through inlet and outlet doors. Materials produced using rotary kilns include Cement, Lime, Refractory's, Met kaolin, Titanium dioxide, Alumina Vermiculite, Iron ore pellets.

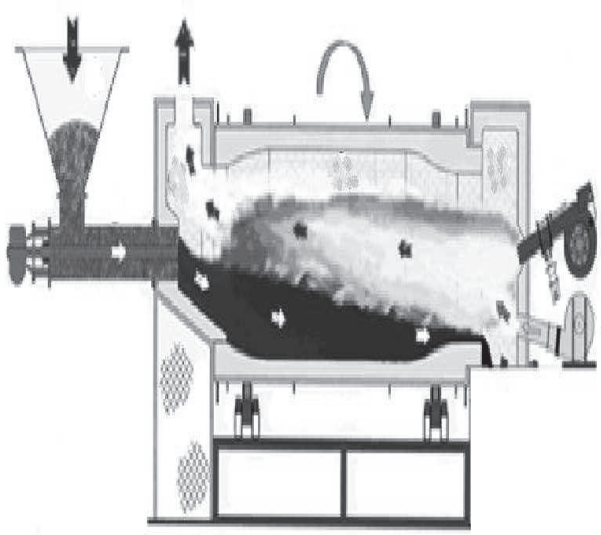

Fig.2 Rotary KILN for DRI process

A typical 500 TPD capacity plant Kiln is 80 m in length and having 4.34 m inner &4.85 outer diameter. The basic components of a rotary kiln are the shell, the refractory lining, support tyres and rollers, drive gear and internal heat exchangers. There are some important components of Rotary kiln.

Reduction process: Six chemical reactions are going through seven junctions of rotary KILN, in the first reaction it produces 2Feo, in the second reaction produces Fe and the final reaction produces satisfactory product 2Feo along with the carbon dioxide. The reactions are taken into the KILN is shown in Table.1

Si. No.	Reaction	ΔG^0_T	ΔG^0_{298}	ΔG^0_{1273}	ΔH^0_{298}	ΔH^0_{1273}
1	$Fe_2O_3 + CO \rightarrow 2\,FeO + CO_2$	+2,120 – 10.39T	-976	-11,106	+2,270	-2,532
2	$FeO + CO \rightarrow Fe + CO_2$	-4,190 +5.13T	-2,661	+2,340	-4,430	-5,808
3	$C + CO_2 \rightarrow 2CO$	-94,200 - 0.2T	-94,260	-94,455	-94,050	-94,561
4	$2CO + O2 \rightarrow 2CO2$	+40,800-41.70T	+28,373	-12,284	+41,210	+39,964
5	$FeO + C \rightarrow Fe + CO$	+36,610-36.57T	+25,712	-9,944	+36,780	+34,277
6	$Fe_2O_3 + 3/2\,C \rightarrow 2Fe + 3/2CO_2$	54,940-62.68T	+36,261	-24,852	+55,225	+50,573

Table1.Thermodynamic data of important reactions. *ΔG & ΔT* in *kCal/Kg*.mole, *T* in o*K*

Kiln & conveyor driving motor: In this paper, 12V DC motor has been used to run the KILN, conveyor belt & Blower fan is shown in fig.3 but in real time all the industries uses three phase induction motors with high power specifications. Specifications of the KILN driving motor (prototype) is shown below table.2.

S.No	parameter	specifications
1	Lubrication	: synthetic, lifetime lubricated
2	Wire terminations	1/4˝ strip
3	Efficiency	up to 75%
4	Shaft	1137-1144crs (standard) 300/400 series
5	Brush life	up to 2,000 hours
6	Bearings	pm iron (standard) pm bronze
7	Insulation	class b (130° c)
8	Voltage rating	6-48 volts dc nominal
9	Leads	16ga awg type gpt (80° c)
10	Rotation	cw, or reversible

Table.2.KILN driving motor specifications

Fig.3 Electrical DC motor

Power Amplifier Circuit: Power amplifier circuits are required to drive a DC motor. This circuit can be shown in Fig.4.This produces proportional amplified signal in order to drive the motor. This signal will be generated by PID controller [5].

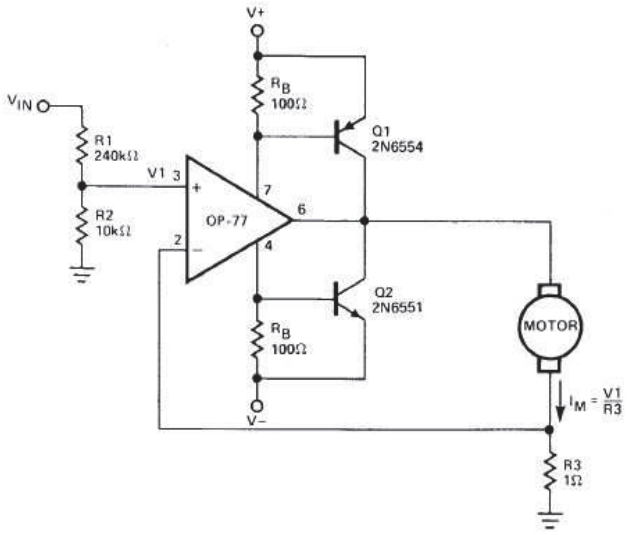

Fig.4 power amplifier circuit

Using a simple operational amplifier and some other common electronic components can be designed a very simple DC motor driver that can be used for a 200mA motor application, which is shown in Fig.4.Rb sets the bias point for transistors Q1 and Q2. Because Vbe (ON) varies greatly with temperature, a guard band is required to prevent Q1 and Q2 from conducting simultaneously. RB should be selected such that the transistors do not conduct until lM equals the op amp quiescent supply current, Isy. The transistors will begin to conduct at about Vbe (on) = 0.5V.

In this circuit:

RB = [Vbe (on)/(lSY+ Im)]

= 0.5/(0.0025 + 0.0025)

= 100 Ohms.

To maximize voltage swing across the motor, V1 must be minimized. If at full load V1 = 0.2V with V+ = 15V and V_{BE1} = 0.8V, the voltage across the motor will be:

V_M = (V+ - 2) - V_{BE1} - V_1

= (15 - 2) - 0.8 - 0.2

= 12.0V

Vin may be scaled with a resistive divider as:
V_{IN}= (R1 + R2)/R2.
With R1 = 240k Ohms and R2 = 10k Ohms, V_{IN} =5 volts, l_M = 200mA.

IV. PROGRAMMABLE LOGIC CONTROLLER

In this paper control operations can be done by PLC. This is used for continuous control applications like DC motor speed control, boiler liquid level control. In view of this PLC analog modules are required to interface electrical motors through power amplifier circuits. In early 1960's most of the industries faced problems in trouble shooting of relay circuits. Once the relay was failed then it takes lot of time to find where the problem occurred. If the production need to be increased then it causes to complexity of wiring through relay contacts .In view of this 1969 Richard Morley introduce programmable logic controllers [6]. PLC is solid state equipment, which was mainly introduced for industrial applications and also for home control applications and which performs logical control actions.PLC programming can be written in different alternative programming formats [7], these are ladder programming, functional block and instruction list.

A. MicroLogix 1200

MicroLogix 1200 expansion I/O (Bulletin 1762) is used to provide discrete and analog inputs and outputs, and specialty modules shown in below fig.5. For the MicroLogix 1200, you can attach up to six additional I/O modules [7]. The number o1762 I/O modules that can be attached to the MicroLogix 1200 is dependent on the amount of power required by the I/O modules

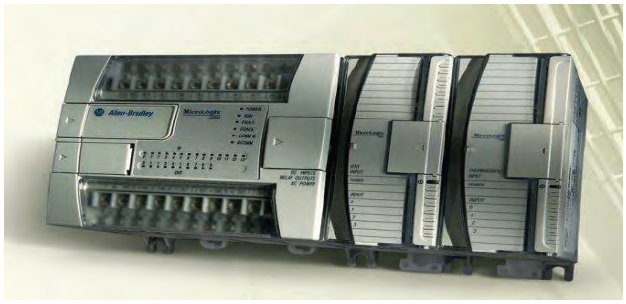

Fig.5 A-B micro logic 1200 PLC

B. Analog I/O Modules of PLC

Analog I/O modules are used to interface analog input signals from the different sensor like Thermocouples, Strain gauges, flow meters and level sensors, which produces analog signals in the form of mvolts or mAmps. These signals will be amplified and given to PLC analog input terminals and then go for scaling process **[7].** In this project thermocouple are used to measure the temperature.

C. Scaling of analog I/O signals

After interfacing of input signals to the PLC input terminals, the signal to be scald into desired values in order to match the PLC instruction parameters. PLC has a programming function to make scaling. Through that functions signal can be scaled into desired parameters [7]. In this paper, Micro logic 1200 PLC is used with compact I/O analog modules (1769-IF4 and 1769 0F2). After scaling the parameters to be included to PID setup is shown in Fig.6

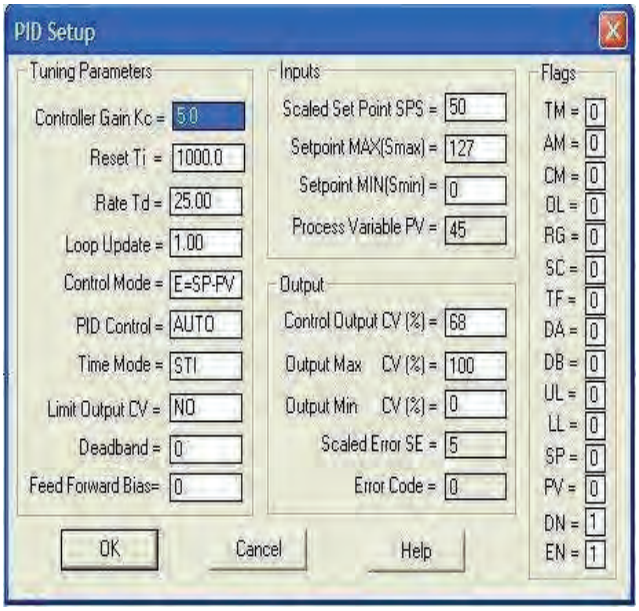

Fig.6.PID controller Setup.

The IF4 has 4 input channels, which are individually configurable (shown in below fig.7). In this example, analog input 0 is configured for 0 to 10V and is scaled in engineering units. Word 0 is not being used in a PID instruction. Input 1 (word 1) is configured for 4 to 20 mA operation with scaling configured for a PID instruction. This configures the analog data for the PID instruction.

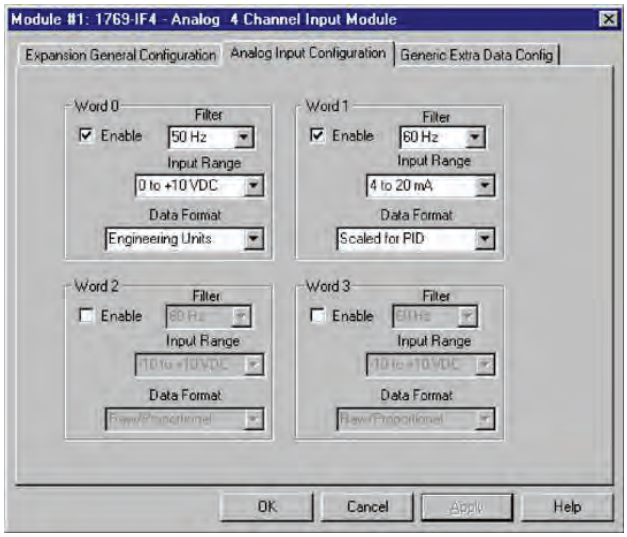

Fig.7.Analog channel configuration

In this paper, Allen-Bradley Micrologix 1200 series – C PLC is used to perform required control actions. Here, PLC analog and digital modules both are required to implement this project and signal conditioning circuits are also needed to drive field devices. Six digital input terminals are required to interface master start and stop buttons of electrical machines [8]. Here two buttons are used for start and stop of rotary KILN, two switches for coal conveyor and two more switches for iron ore

conveyor belt. Two analog input terminals are required to interface K type thermocouples and two analog outputs are required to drive conveyor DC motors. If indication is required then more digital terminals are required.

D. Operational procedure

This paper describes the control of DRI process with the aided of PLC. In this process the iron ore is converted into sponge iron at different temperature ratings with respect chemical reactions [8]. The quality of product depends on temperature ratings at the KILN junctions. So, temperature has to be controlled in order to get high quality of product. Whenever process is started then the temperature at the junctions will be measured by thermocouples and which are interfaced to PLC analog input modules, this value is calibrated into temperature degree Celsius and displayed on SCADA screen.

PLC PID controller sends control signals to coal conveyor and blower fan by considering junction temperature in order to maintain desired temperature at the KILN junctions. Here, we need to develop the program for this control operation using PLC PID functions by considering controller tuning methods. If the temperature exceeds the desired values then the PLC sends the control signals to blower fan and coal conveyor then the speed of conveyor belt on blower fan either decreased or increased until reached the desired value. The controlling operations can be taken by user from the SCADA system and we can also monitor the status of process on SCADA screen. The designed project is shown in the below fig.8.

Fig.8.Designed project (Hardware equipment)

E. Tuning of controller

Tuning is the process of selecting the best parameters of controller. In this paper we are using Ziegler-Nichols PID tuning method. This is the methods for finding proper values of Kp, Ti and Td.

While tuning is going, mainly four parameters should be considered, these are settling time, off set, good stability and overshoot. Here Kp, Ki and Kd values should be tuned until to get the good stability and response of the process is shown in Fig.9. If the damping ratio is very high then the response of the system is very slow, so which takes a lot of time to reach the set point. If the damping ratio is zero then it produces continuous oscillations then the system will go to instability conditions, which causes to damage of final control element [9]. If the damping ratio is less than 1 then it produces under damped response, which is very speed response but poor stability. If the damping ratio is 0.5 then it has acceptable stability and medium fastness.

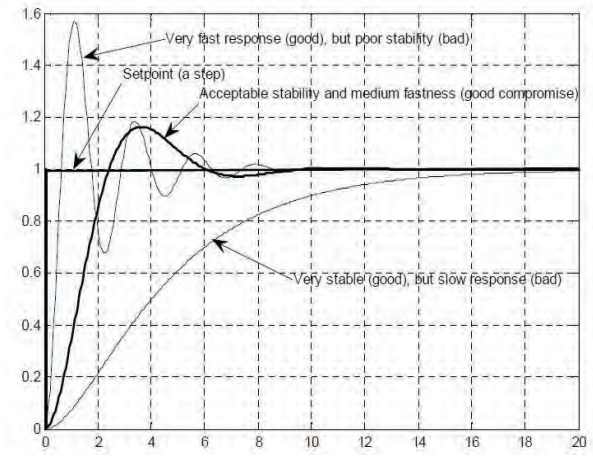

Fig .9: In controller tuning we want to achieve this compromise: Acceptable stability and medium fastness of response

V. THE ZIEGLER-NICHOLS' PID TUNING PROCEDURE

In this paper, DC motor to be controlled by the PLC-PID controller [9], so PID controller parameters have been tuned in order to get good response of the system. To find the best parameters of the controller The Ziegler-Nichols' closed loop method is based on experiments executed on an established control loop (a real system or a simulated system), shown in Fig.10.

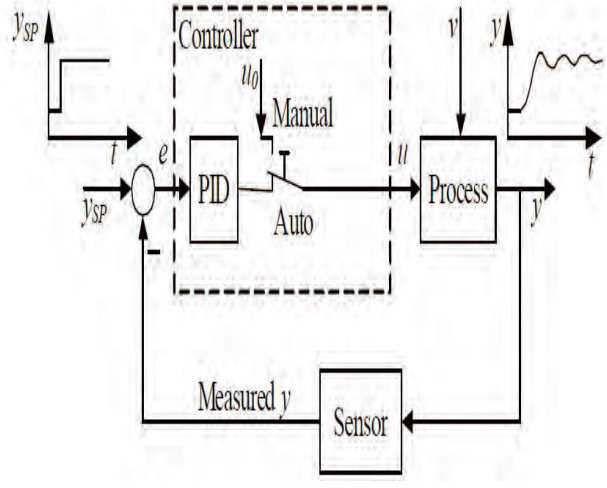

Figure.10: closed loop The Ziegler-Nichols' tuning method

The tuning procedure is as follows:

This method is primarily experimental & uses real process data from the systems response. This method was developed by Ziegler & Nichols, which is based on frequency response analysis. Unlike process reaction curve method which uses data from the Open loop response of a

system, the Ziegler – Nichols Technique is a closed loop procedure.

In this method, first, bring the process to the desired operational level and then, use proportional control only with the feedback loop closed by vending the proportional gain until the system oscillates continuously & let that proportional gained Kc & period of Oscillations as Pu. By using the following recommended settings for feedback. Controller given by Ziegler & Nichols calculates the controller settings.

Table2: tuning parameters for P, PI, PID controllers

Controller	K_c	T_{int}	T_{Der}
P	$K_{c/2}$		
PI	$K_c/2.2$	$P_u/1.2$	
PID	$K_c/1.7$	$P_u/2$	$P_u/8$

A. Input and output configuration with RS- Logix 500

After the completion of PLC programming, before going to dumping or downloading. We should read I/O configuration of PLC. Once read I/O configuration then automatically detects PLC, which is interfaced to PC [RS-Logic 500].Which makes a path to dumping the programming to PLC. Here configuring is done automatically or manually. Once you open RS Logic 500 and then make double click on read I/O configuration then automatically shows different series of PLCs after that we need to select PLC series which has been interfaced to PC. After that write PLC programming into selected PLC and then go to RUN mod to monitor the status of I/O devices.

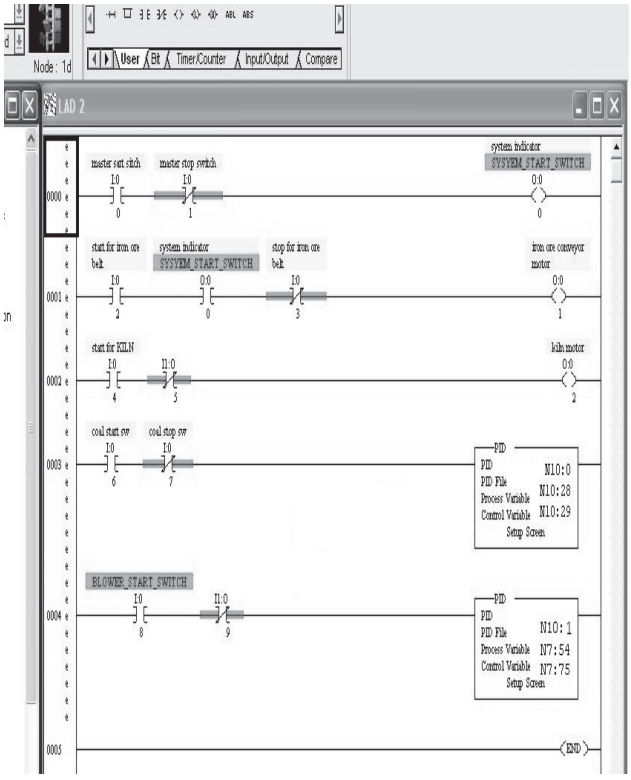

Fig.11.PLC program for the project

The following instructions are the desired PLC programming instructions to write the program [1].

1. Normally open
2. Normally closed
3. PLC PID function
4. Arithmetic Functions

Addressing format

Input->I: 0/3, I: 0/2, I: 0/5, I: 1/0, I: 1/3

Output->O: 0/0, O: 0/1, O: 1/0, O: 2/4

VI. SCADA AND RESULTS

The status of field devices can be monitored and controlled by SCADA system [5]. In view of this Field devices and SCADA is interfaced through the PLC. RS View32 SCADA is used in this project.

Follow the steps below to link up PLC with RS VIEW32:

1. Go to Start and open RS VIEW SCADA software.
2. Click on File and create a new project by clicking on New. After creating a new project, the options available in the project manager
3. Go to system and double click on channel. In the Channel editor, select a channel and assign the appropriate network type to it as shown in figure.12. In the Primary Communication driver field [10], assign a driver to the channel. If you do not have drivers loaded, click None Loaded. For example, select DH-485as the network type, select the Primary Communication Driver as AB-DF1-1 and select the check box primary for active driver.

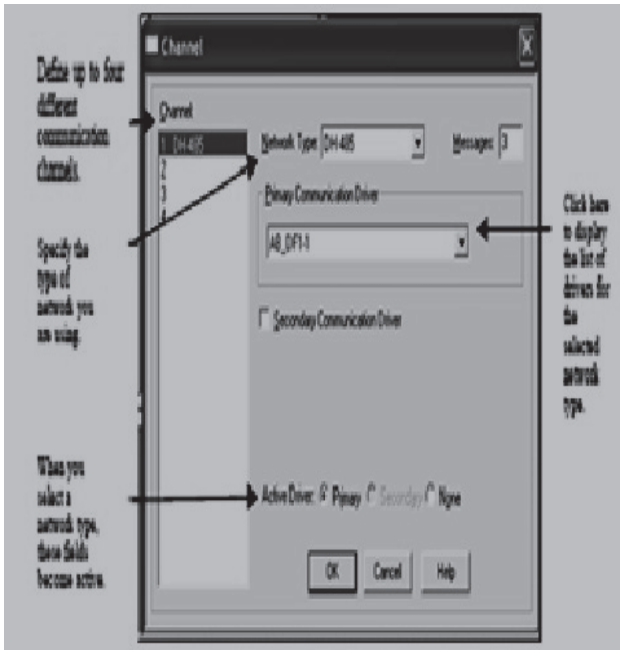

Figure 12: Configuring Channel for Direct Driver Communication

4. Create nodes according to the number of inputs and outputs required in the program. For each node assign the station by clicking the station browse option. The figure .12 shows the typical dialog box for creating nodes.

5. Accept after creating each node and click next so as to add each and every node.

6. Go to tag database after completing the nodes.

7. There are two ways by which tags can be created. The first way is in the Tag Database editor to Create tags [10]. For each tag, select Device as the data source and assign the nodes and scan classes that you have defined. The tag database dialog box is shown in figure 13.

8. Now in tag database, add the name, type and security of tags one by one. Choose either device or memory depending on for what we are creating the tags.

Figure 13: Creating tags using Tag Database

9. If device is chosen i.e., if we are taking the field devices and connecting to PLC then we need to choose device and give proper addressing format with its scan class and attach them to specific node.

10. After each tag, presses accept to save and then next to proceed to other tags.

11. Go to graphics and open display. Create the inputs and outputs in the white display with the help of library.

12. Right click on each element and select animation and supply visibility, color, rotation, fill etc. as required by the user. For each animation, tags have to be imported by browsing from the tags.

13. After the animations are done for each and every object according to the program, save the display and it can be retrieved from the library again.

14. After saving, run both the PLC ladder program [10] and test u run for the SCADA screen created. We see that the current state of the inputs and output buttons or field devices is reflected on the screen at every instance.

***SCADA results*:** Open the project file in the Rs View 32 software [5] then click on the then select the project file which is already designed .This page explains that it is a home screen for total project. This is shown in Fig.14.

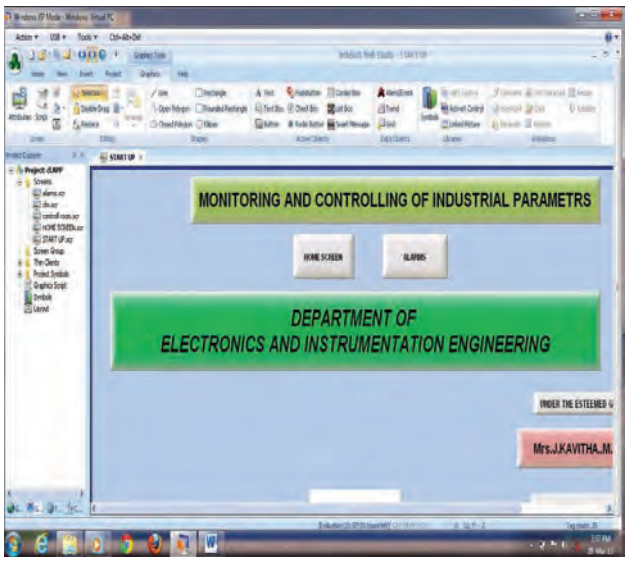

Fig .14.SCADA Home screen of the project.

Then click on the home page then a wizard is open as follows. It describes that this is the complete animated representation of total project is shown in fig.15. .Hence the total process can be monitored and controlled here.

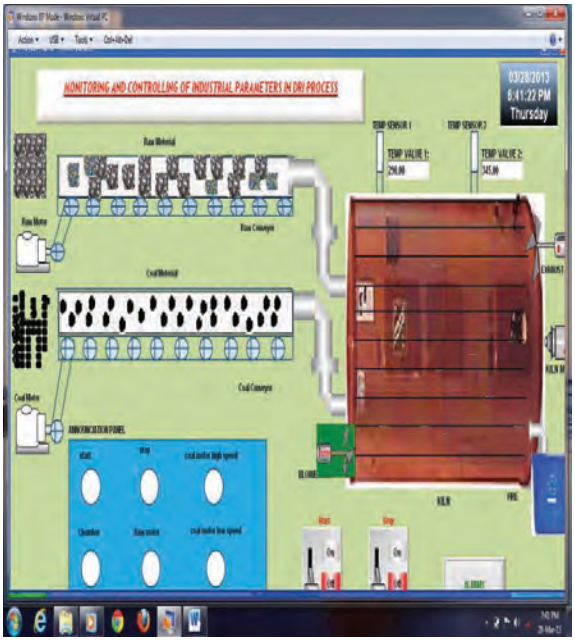

Fig.15.Total project representation through SCADA

VII. CONCLUSIONS

The use of SCADA Based Automatic Direct Reduction of Iron (DRI) Process Using Allen-Bradley PLC is an advantage over the traditional control systems as the monitoring and controlling can be done without human intervention. Quality of production of iron can be increased by this automation process. This automatic process linearly changes the field parameters (like feed rate of raw material, inlet and outlet pressures) with respect to desired product quality.

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Multi-Channel UART Controller with FIFO and FPGA

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Abstract—**Communication between the complex control systems can be done by a multi-channel UART controller based on FIFO (First In First Out) technique and FPGA (Field Programmable Gate Array).The communication between the master equipment and slave equipment with different baud rate can be done by using this controller. This controller consists of a FIFO circuit block and UART circuit block. In this controller an asynchronous FIFO is used. The design method of an asynchronous FIFO is also presented. A universal Asynchronous Receiver-Transmitter usually (UART) converts data from parallel to serial and serial to parallel. It operates on any two independent clock domains.**

Index Terms: FIFO, FPGA, UART**.**

I. INTRODUCTION

In serial communication, a UART (universal asynchronous receive/transmit) plays an important role. A universal asynchronous receive/transmit (usually abbreviated UART) has a transmitter section and a receiver section. The distortion of a signal can be reduced in serial communication. Serial communication is preferred for long distance transmission. Parallel communication requires multi- bit address bus and data bus, and it is implemented for short distance transmission. We have a parallel or serial port, and the communication between any two systems may be serial or parallel communication. If the Master Control Unit (MCU) is sending or receiving the data at one baud rate and the sub-equipments are receiving or sending the data at another baud rate then there is a possibility of loss of data. To overcome this problem, an asynchronous FIFO is placed between MCU and sub-equipments. In designing a FIFO, Gray code is used for addressing the memory locations. The advantage of Gray code is that there is only one bit change in the address of the successive address memory location. This will overcome the Met-stability condition [1]. An asynchronous FIFO has either full or empty condition. FIFO is an important part of these systems and it acts like a link between the devices.

The features of multi-channel UART controller depend on the asynchronous FIFO. The communication between the MCU and the multi-sub equipments is shown in the below figure.1. The MCU baud rate is different to that of the sub-equipments. The baud rates of the sub-equipments are different to each other. A special baud rate converter is used to implement the communication between the MCU and the sub-equipment.

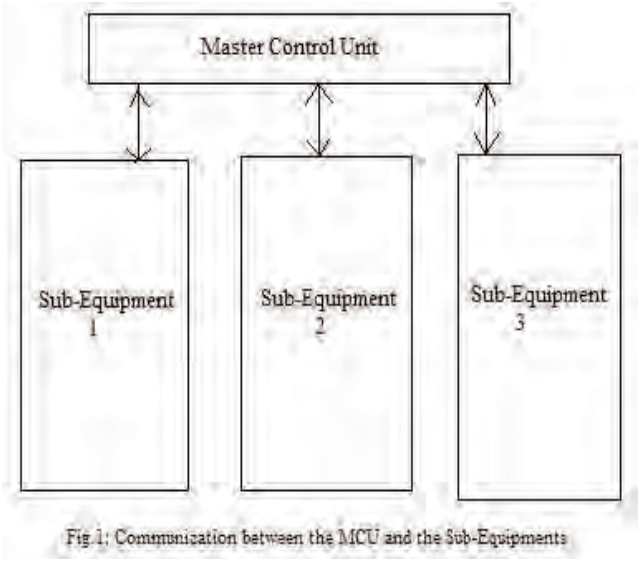

Fig.1: Communication between the MCU and the Sub-Equipments

II ASYNCHRONOUS FIFO DESIGN

A. Connections of an asynchronous FIFO

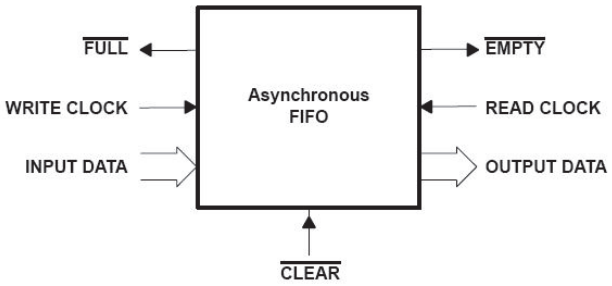

Fig.2. Connections of an asynchronous FIFO

In an asynchronous FIFO, the data is written based on the write clock pulse and the data is read based on the read clock pulse. The two operations in an asynchronous FIFO are read and write as shown in fig.2. The write and read operations takes place for two different clock domains. The status of an asynchronous FIFO can be determined by the FULL and EMPTY signals. When the FIFO is full there is no space for writing the data. When the FIFO is empty there is no data to read. The clear signal is used to erase the data in an asynchronous FIFO.

B. ASM chart of an Asynchronous FIFO

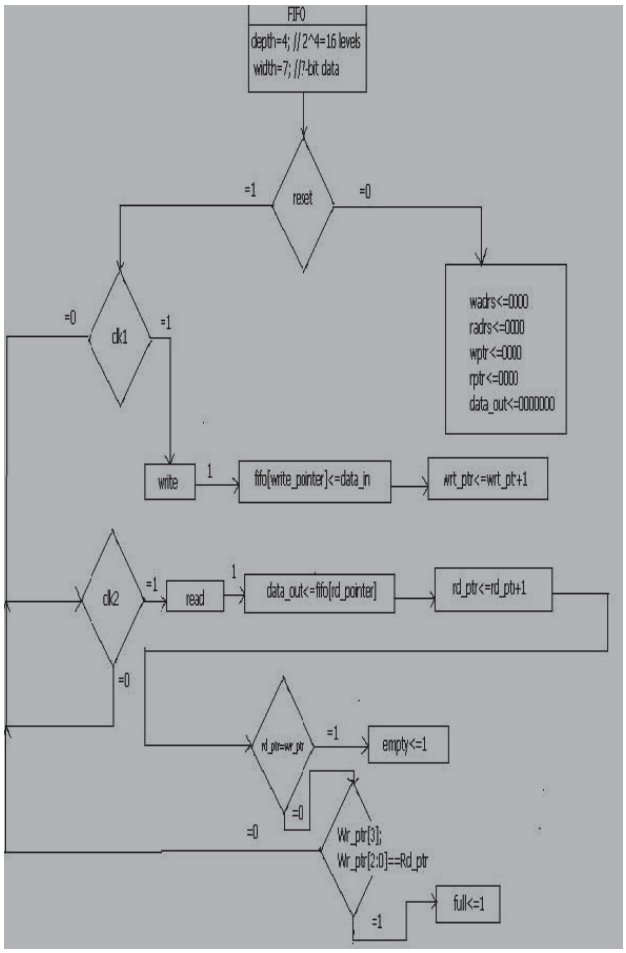

Fig.3: ASM chart of an Asynchronous FIFO

FIFOs are often used to safely pass data from one clock domain to another asynchronous clock domain. Using a FIFO to pass data from one clock domain to another clock domain requires multi-asynchronous clock design techniques [1].

An asynchronous FIFO refers to a FIFO design where data values are written to a FIFO buffer from one clock domain and the data values are read from the same FIFO buffer from another clock domain, where the two clock domains are asynchronous to each other. To determine full and empty status for an asynchronous FIFO design, the write and read pointers will have to be compared. If a reset or read makes the pointers equal to each other, the FIFO is really empty. If a write makes the pointers equal, the FIFO is full [1].

The ASM chart of an asynchronous FIFO is shown in the above figure.3. In this asynchronous FIFO, the numbers of memory locations are 16 and in each memory location 7-bits of data can be stored. When the reset control signal is 0, the write addresses, read address, write pointer, read pointer and data out are rested to zeros. When the reset control signal is 1,it checks the clock1 signal. If the clock1 signal is 1, then the write operation takes place. If the clock1 signal is 0, it checks the clock2 signal. If the clock2 signal is 1, then read operation takes place. When the clock2 signal is 0, again it checks the clock1 signal. If the read pointer and the write pointer points out to the same memory location, the FIFO is empty. If the MSB bit of write pointer is not equal to the MSB bit of read pointer and the remaining bits are equal then the FIFO is full.

C. Logic Involved in an asynchronous FIFO

Asynchronous FIFOs are used to safely pass data from one clock domain to another clock domain. Asynchronous refers to two different clock domains. The Master Control Unit (MCU) sends the data to FIFO at one clock domain and the sub-equipments receive the data from the FIFO at anther clock domain. A method is presented that is used to design, synthesize and analyze a safe FIFO between different clock domains using Gray code pointers that are synchronized into a different clock domain before testing for FIFO full‖ or FIFO empty condition [2]. For a FIFO design, we require the full component, empty component, and synch module component. In a FIFO, the data is written at clock1 frequency and the data is read at clock2 frequency. To determine full and empty status for an asynchronous FIFO design, the write and read pointers will have to be compared.

The FIFO is in full condition when

WPtr (4)/=WSync_rptr (4) and WPtr (3) /= WSync_rptr (3) and WPtr (2 downto 0) = WSync_rptr (2 downto 0).

The FIFO is in empty condition when

rptr = rsync_wptr

To avoid metastability, Gray code is used as an address of each memory location instead of binary code. The probability of occurrence of an error is very low by using Gray code.

The conversion between the Binary codes and the Gray codes is as following [3]:

$g_n=b_n$

$g_i=b_i \text{ Xor } b_{i+1} \quad i\neq n$ and

$b_n=g_n$

$b_i=g_i \text{ Xor } b_{i+1} \quad i\neq n$

D. Simulation result of an Asynchronous FIFO

Rst: When the control signal rst is _0‘ no operation takes place and when the control signal rst is _1‘ the write operation and read operation takes place, which is shown in Fig.4.

Clk1: When the control signal clk1 is _1‘ then write operation takes place.

Clk2: When the control signal clk2 is _1‘ then read operation takes place.

Radrs [3:0]: This control signal indicates the address of the memory location from where the data can be read.

Wadrs [3:0]: This control signal indicates the address of the memory location to which we can write the data is shown in Fig.4.

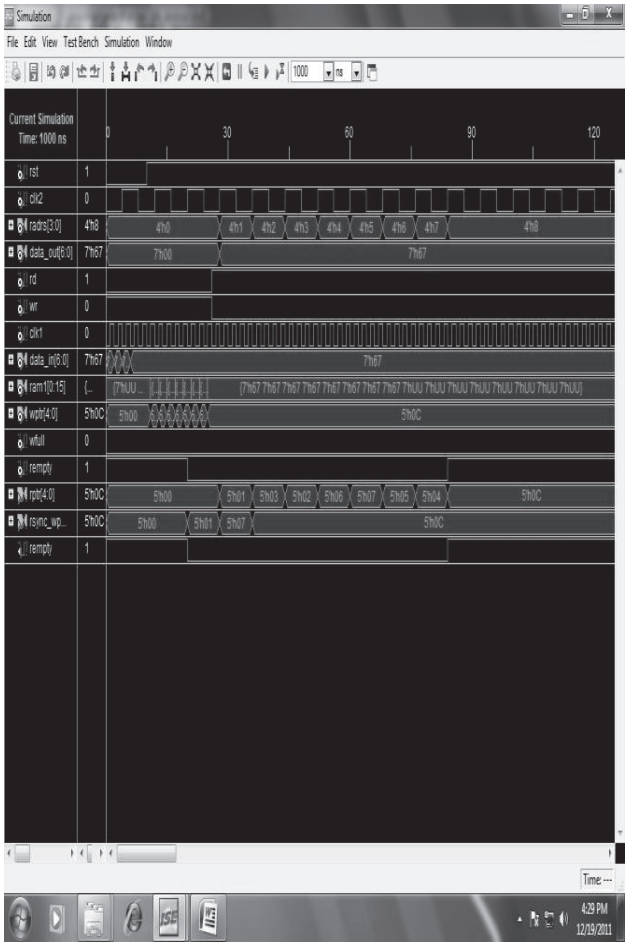

Fig. 4: Simulation result of an asynchronous FIFO

Data_out [6:0]: This control signal indicates the output data. The output data can be observed on the bus channel 21, bus channel 22, and the bus channel 23.

Rd: If the control signal rst is _1‘, clk2 is _1‘ and the rd is _1‘ then the read operation takes place.

Wr: If the control signal rst is _1‘, clk1 is _1‘and the wr is _1‘then the write operation takes place

Data_in [6:0]: This control signal indicates the data to be transmitted from the MCU to the Subs. The data can be observed on the bus channel 1.

Ram1 [0:15]: It is a part of a FIFO and it contains 16 memory locations. The data is placed in each of the memory location.

Wptr [4:0]: This control signal points out the memory location where the data can be written.

Rptr [4:0]: This control signal points out the memory location where the data can be read.

Wfull: If this control signal is _1‘ then the FIFO is full.

Rempty: If this control signal is _1‘ then the FIFO is empty.

E. ASM chart of UART Transmitter:

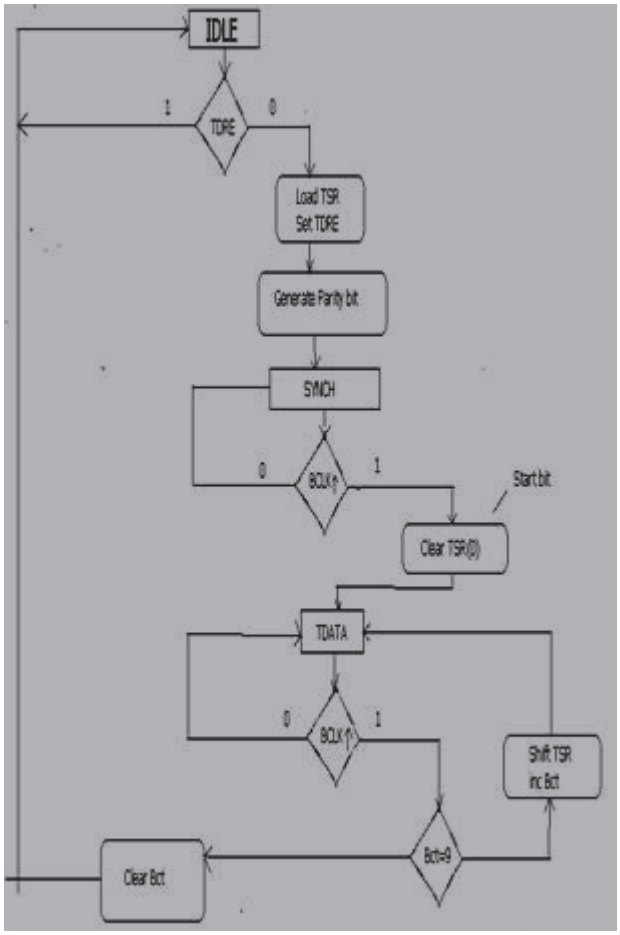

Fig.5: ASM chart of UART Transmitter

The UART circuit block consists of three parts Transmit circuit, Receive circuit and Control/Status registers. The transmit circuit consists of a transmit buffer and a shift register. If rst_n=1,wr=1 and txrdy=1 then tx_sts=1.

If transmitter is ready, then we need to load data from data line to data buffer register. A parity bit is also generated in order to check whether the received bits are correct or incorrect. If TBR (Transmission Buffer Register) contains data then a parity bit is generated by Exclusive operation of all the bits in TBR[3]. A start bit, data bits, a parity bit and a stop bit are loaded into TSR. For every four clock pulses, a baud clock is generated. Each baud clock pulse is used to transmit the data in TSR bit by bit.

The source code which is used to describe the UART transmitter as shown in Fig.5 consists of

(a) A module indicating the transmitter status.

(b) A module which is used for loading the data from data line to TBR.

(c) A module which is used for generating a parity bit..

(d) A module which is used for generating a baud clock.

(e) A module which is used to shift the bits in TBR to TSR bit by bit.

F. Logic Involved in UART TRANSMITTER

The UART circuit block consists of three parts Receive circuit, Transmit circuit and Control/Status registers. The transmit circuit consists of a Transmit Buffer and a Shift Register. Transmit Buffer loads data being transmitted from local CPU. And Shift Register accepts data from the Transmit Buffer and send it to the TXD pin one by one bit. When a control signal tx_sts=1 then the transmitter is busy. The TBR can load the data of 7 bits. When the control signal txrdy=1, then we need to load data from data line to data buffer register . A parity bit is generated, whenever data is present in TBR. The logic involved for generating a parity bit is —the bits in TBR are XORed [4].

Parity bit = tbr(0) XOR tbr(1) XOR tbr(2) XOR tbr(3) XOR tbr(4) XOR tbr(5) XOR tbr(6)

For every four clock pulses a baud clock is generated. For each baud clock a bit is transmitted from TSR to the receiver circuit. The TSR can load the data of 10 bits. In the TSR, the first bit indicates start bit, the ninth bit indicates the parity bit, and the tenth bit indicates the stop bit and from the second bit to the eight bit indicates the bits from TBR. When TSR contains no data then txrdy=1 which indicates that the entire data has been sent to the receiver circuit.

G. Simulation Result of UART Transmitter

The simulation result of UART transmitter is shown in Fig.6. The UART block consists of a transmitter section and receiver section. The transmitter consists of TBR and TSR (Receiver Shift Register). The receiver section consists of RBR (Receiver Buffer Register) and RSR. The TBR consists of 8-bits of data. The TSR consists of start bit, stop bit, parity bit and 8-bits of data. The bits in TSR are shifted to RSR bit by bit. The data bits in RSR are shifted to RBR.

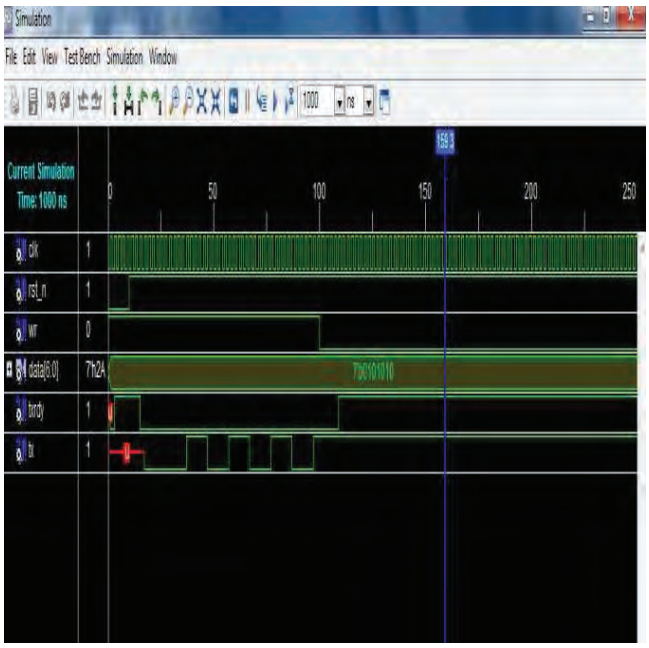

Fig.6: Simulation result of UART Transmitter

Txrdy: If this control signal is _1‘ then TSR has finished in sending the data. If this control signal is _0‘ then TSR has data to be sent.

Tx: This control signal indicates the data that is to be transmitted to the sub-equipments. The data is transmitted to the sub-equipments at different baud rates.

Wr: It is a control signal which indicates the write operation.

Rst_n: This is a control signal which indicates the reset operation.

H. ASM Chart of UART receiver

The ASM chart of UART receiver is shown in Fig.7.

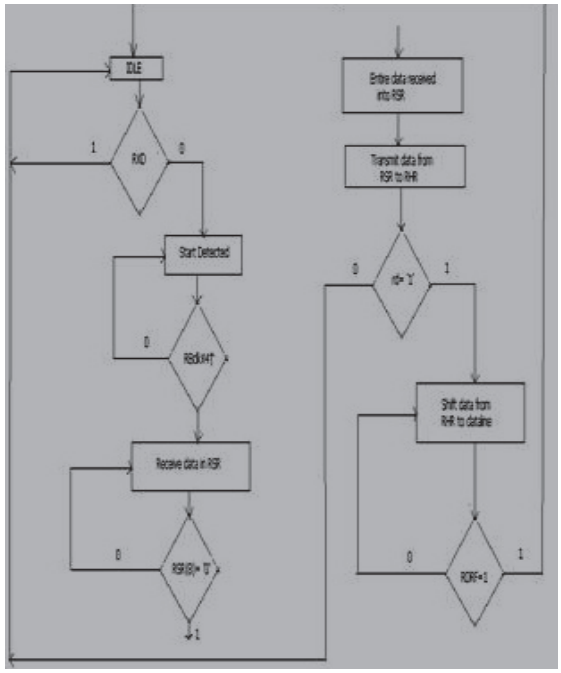

Fig.7: ASM chart of UART receiver

The UART circuit block consists of three parts receive circuit; transmit circuit and control/status registers. The receive circuit consists of a receive shift register and a receive buffer. If a start bit is received into RSR then the control signal det_rx is enabled as shown in Fig.7. The bits in the TSR(Transmitter Shift Register) are shifted bit by bit into the RSR(Receiver Shift Register). If the start bit occupies the first position or first bit of RSR then all the bits are received into receiver. The RSR is reset i.e., RSR contains all 1s. For every four clock pulses, a baud clock is generated. Each baud clock is used for receiving one bit. If the first position of RSR contains _0‘ then the data bits in RSR are shifted into the RHR(Receiver Hold Register). If the read, rd control signal is high then the data in RHR is shifted to data line. The status of the receiver whether it is ready or not can be determined by the control signal rxrdy. If the first position of RSR contains _0‘ then the receiver is ready. If the above condition is not satisfied the receiver is not ready.

I. Logic Involved in UART RECEIVER

The UART circuit block consists of three parts Receive circuit, Transmit circuit and Control/Status Registers. The receive circuit consists of a Receive Shift Register and a Receive Buffer. The Receive Shift Register receives data from RXD one by one bit. The Receive Buffer loads data from long-distance MCU and gets it ready for the local PC to read. If the start bit _0‘ is received, det_rx control signal is enabled. If the start bit _0‘ occupies the first position of RSR then all the bits are received into the receiver. For each four clock pulses a baud clock is generated. Based on the baud clock the bits are received from the transmitter circuit. The bits in RSR are shifted to the RHR except the first and the last bits. When the control signal read (rd=‘1‘), the data is shifted from RHR to data line.

J. Simulation result of UART receiver

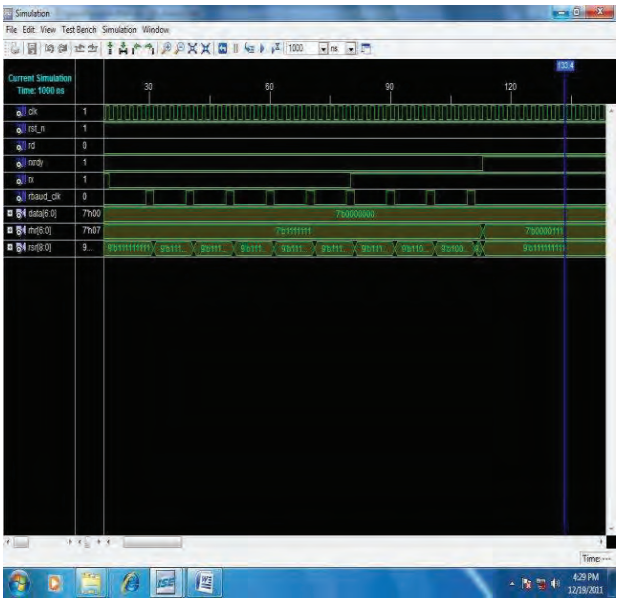

Fig.8: Simulation result of UART receiver

Clock: When the control signal clock is _1 then the receiver is ready to accept the data.

Rst_n: When the control signal rst_n is _0 no operation takes place and when it is _1‘ the data receiving operation takes place.

Rd: When the control signal rd is _1 then the data in

RHR can be read into the data line as shown in Fig.8.

Rxrdy: This control signal indicates whether the receiver is ready or not.

Rx: This control signal indicates the data to be received from the data line to the RSR.

Rbaud_clk: When this control signal is _1‘ then the data is received from the transmitter line to receiver i.e., to RSR as shown in Fig.8.

Data [6:0]: This control signal indicates the input data.

Rhr [6:0]: This control signal indicates the data in the Receiver Hold Register.

Rsr [8:0]: This control signal indicates the start bit, the data bits and the stop bit.

III. IMPLEMENTATION OF A M-CHANNEL UART CONTROLLER

In the multi-channel UART controller, there are various blocks which includes UART block, status detectors, asynchronous FIFOs block and baud rate generator block. All the blocks in the controller has its own function. The main part is UART circuit block and its structure is shown in figure. The communication between any two devices is broadly classified into two types i.e., the serial communication and the parallel communication. In serial communication, the data bits are transferred bit by bit whereas in parallel communication, all the bits are transferred at a time. Parallel communication requires less amount of time and serial communication requires more amount of time for transferring the data. The cost of parallel communication is more compare to the serial communication. If the communication is within the system then the parallel communication is preferred. Suppose, if the communication is between any two systems separated by a great distance then the serial communication is preferred. The UART block is used for converting serial data to parallel data and vice-versa. Asynchronous communication between any two systems will occur when the two systems are operating with different clock domains.

In asynchronous communication, a start bit, a stop bit, a parity bit and the data bits are used. The start bit indicates the start of communication between any two systems. After the start bit, the data or message bits are sent. For detecting the error, a parity bit is sent from the transmitter section to the receiver section. The parity bit

may be an even parity or odd parity. The stop bit indicates the end of communication between any two systems.

A.UART Architecture

The main functional blocks of an UART as shown in below Fig.9 are:

CPU Bus Controller

Baud rate generator

Receiver /Transmitter

CPU Bus Controller

A bus is a group of wires. The bus is classified into three types. They are control bus, data bus and address bus. The bus controller controls these buses. The control bus is used for transmitting the control signals like bus request, bus grant, hold request, and hold acknowledge etc. The data bus carries the data bits from one block to the another block. The address bus carries the addresses of various memory locations in the memory.

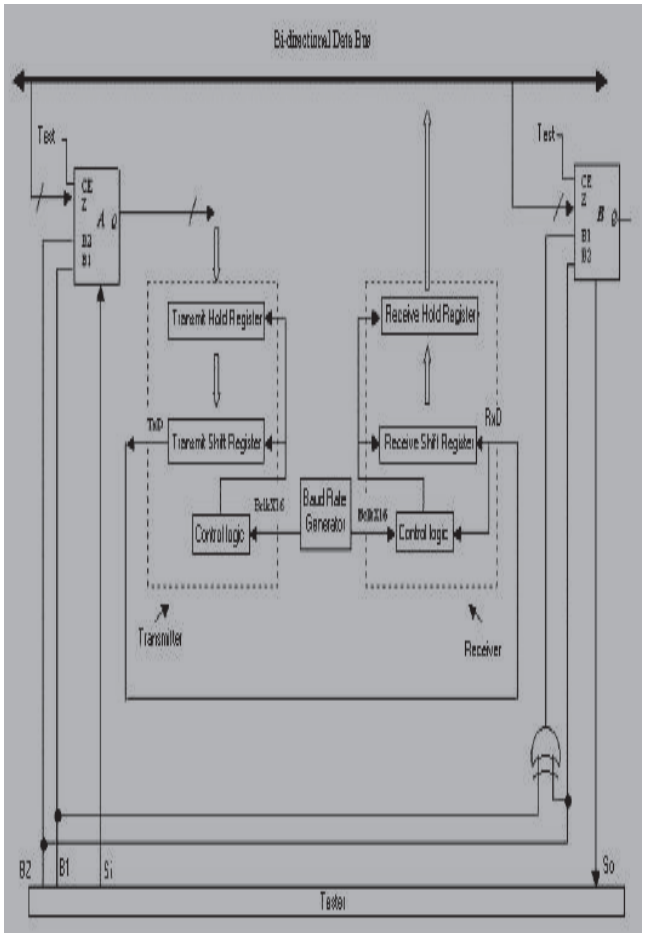

Fig.9:UART block diagram

Baud rate generator

The purpose of the baud rate generator is to generate the baud rate signals. The baud rate indicates the number of bits per second i.e., the transmitter section can send and the receiver section can receive. In UART there are two main blocks i.e., the transmitter section and the receiver section. The baud rate generator is connected to the transmitter section as well as to the receiver section. Based on the baud rate, the transmitter section sends the bits to the receiver section and the receiver section receives the bits from the transmitter section. By suitable selection of the baud rate, the bit loss can be overcome between the transmitter and the receiver section.

Receiver /Transmitter

The transmitter section of an UART block consists of a Transmitter Hold Register (THR) and Transmitter Shift Register (TSR). The receiver section of an UART block consists of a Receiver Hold Register (RHR) and Receiver Shift Register (RSR).The data on the bi-directional data bus is loaded into the THR of the transmitter section of UART.The data bits in THR are loaded into TSR and a start bit, a stop bit and a parity bit are added. These bits are shifted to RSR bit by bit. The RSR contains the data bits, the start bit, the stop bit and the parity bit. Only, the data bits in RSR are loaded into the RHR. The RHR contains the data or message bits.

B.ASM chart

The ASM chart of multi-channel UART controller is shown in Fig.10.The bits are loaded from MCU to RSR. The bits in RSR are loaded to RBR. Here, the RBR contains only the data bits. The bits in RBR are shifted to TBR and the bits in TBR are shifted to TSR. The bits are transmitted to the sub-equipments through the TxD pin. The FIFO is in full condition, when all the bits in wr _ptr are equal to the bits in rd_ptr except the MSB bit of wr_ptr.If all the bits in rd _ptr are equal to all the bits of wr_ptr, then the FIFO is in empty condition.

The UART consists of transmitter section and receiver section. The transmitter section consists of TBR (Transmit Buffer Register) and TSR (Transmit Shift Register).The receiver section consists of RBR (Receiver Buffer Register) and RSR (Receive Shift Register).The purpose of the UART is to convert the data from serial to parallel and parallel to serial. The communication between the Master Control Unit (MCU) and the Sub-equipments is performed by using the multi-channel UART controller. If the Master Control Unit (MCU) is sending the data at high baud-rate and the sub-equipments are receiving the data at low baud-rate then there will be the loss of data. This difficulty can be over commend by using an asynchronous FIFO between the Master Control Unit (MCU) and the sub-equipments. The asynchronous FIFO operates at two different clock domains. The data is read from the Master Control Unit (MCU) at one clock domain and the data is written into the sub-equipments at another clock domain. The MCU and the sub-equipments both contain the UART. The transmitter section of the UART in Master Control Unit (MCU) transmits the data to the sub-equipments and the receiver section of the UART in the sub-equipments receives the data. The Transmit Buffer Register (TBR) in the transmitter section of UART consists of data bits. The start bit, stop bit and a parity bit are added to the data bits and loaded into the Transmit Shift Register (TSR).The bits in Transmit Shift Register (TSR) are transferred into the Receiver Shift Register (RSR) of the receiver section of the

UART in the sub-equipments. Only the data bits in the Receiver Shift Register (RSR) are transferred into the Receiver Buffer Register (RBR) of the receiver section of the UART in the receiver section of the sub-equipments. The communication between the Master Control Unit (MCU) and the sub-equipments is described in the form of ASM chart as shown in Fig.10.

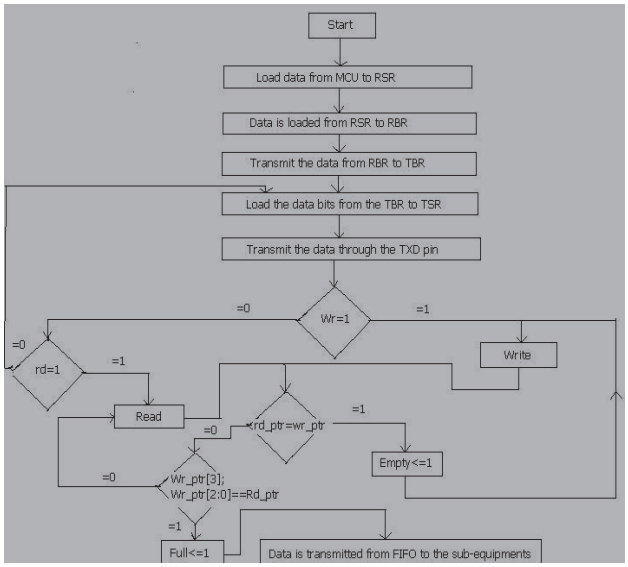

Fig.10.ASM chart of multi-channel UART Controller.

C. Block Diagram

The block diagram of a multi-channel UART controller is shown in the below figure. The communication between the Master Control Unit (MCU) and the sub-equipments is done through the FIFO as shown in Fig.11. If the baud rate of Master Control Unit (MCU) and the sub-equipments are different to each other, then there is a possibility of data loss. This can be overcome by using a FIFO in between the MCU and the sub-equipments. The bus channel 1 is used to transmit the data from MCU to the FIFO s and the bus channel 21, bus channel 22, and the bus channel 23 is used to transmit the data from the FIFO s to the sub-equipments. The UART block is used for converting serial to parallel and parallel to serial data

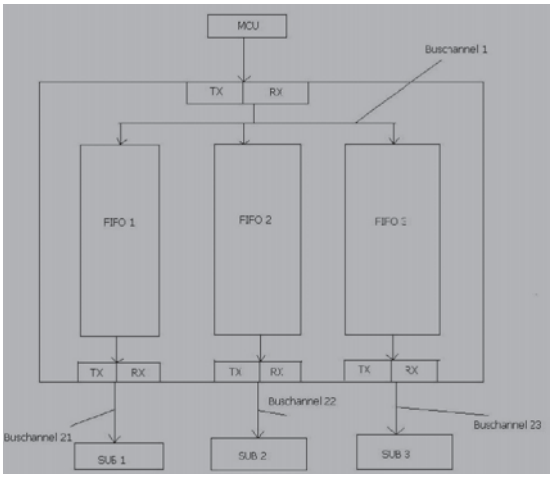

Fig.11.Block Diagram of Multichannel UART Controller.

D. Simulation Result

The simulation result of the top module is shown in the below figure.12. A multichannel UART controller is used for transmitting the data between the master equipment and the three sub-equipments. If the master equipment is sending the data at one baud rate and the three sub-equipments are receiving the data at different baud rates then there will be loss of data. To overcome this difficulty, we are using a FIFO in the controller. A FIFO can store the data and the data can be used latter by the sub-equipments. The structure of the controller consists of UART block, baud rate generator, status detector, FIFO and status buffer. The structure of UART block consists of Transmit Buffer Register (TBR), Transmit Shift Register (TSR), Receiver Buffer Register (RBR), and Receiver Shift Register (RSR).In the simulation description the input data exists on data_in and the output data exists on data_out[5]. The three sub-equipments will receive the data at different baud rates. This can be observed in the simulation diagram where they are labeled as tx. The baud rates of the three transmitters are also different[6]. The simulation result of the controller can be observed below.

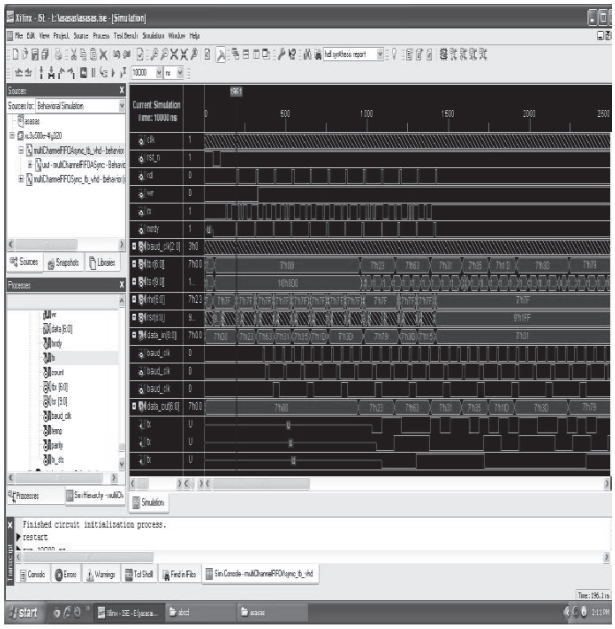

Fig.12.Simulation result of multichannel UART controller (Top module**).**

IV. CONCLUSIONS

This project introduces a method to design an asynchronous FIFO based on FPGA and using an asynchronous FIFO technique implements a multichannel UART controller within FPGA. The controller can be used to implement communications in complex system with different baud-rates of sub-controllers. And it also can be used to reduce time delays between sub-controllers of a complex control system to improve the synchronization of each sub -controller. The controller is reconfigurable and scalable.

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Attacks and Countermeasures on Routing Protocols in Wireless Sensor Networks: A Survey

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Abstract - **Security in Wireless Sensor Networks has become one of the most relevant research topics. Designing a secure routing protocol in a wireless sensor network is a challenging task because of the limitations on memory, computational and communication capabilities, bandwidth and energy of the sensor nodes. Most of the routing protocols that were proposed were designed by keeping efficiency of energy in view but not security. Routing protocols in wireless sensor networks are susceptible to various types of attacks such as hello flood attack, Sybil attack, sink hole attack, worm hole attack, selective forwarding attack, eavesdropping, acknowledgment spoofing, routing table overflow and so on. In this paper we discuss different types of attacks on routing protocols in detail and also some of the defensive techniques proposed in literature to counter the attacks.**

Index Terms - **Wireless sensor network, Routing protocols, attacks, countermeasures**

I. INTRODUCTION

A Wireless Sensor Network (WSN) is a spatially distributed heterogeneous system consisting of one or more base stations and low-powered, low-cost tiny sensor nodes(SNs) capable of sensing, detecting, and monitoring the physical attributes of the environment like pressure, temperature, sound, vibration, acceleration, velocity, humidity, stress, strain and so on. WSNs were initially introduced for military applications, over time the range of applications has been increasingly diversified ranging from defense to general security.

The main task of a sensor node is to sense the data from the environment and communicate it to the base station. The components and the functionality of a sensor node are shown in Table I.

Table I Components of a sensor node

Component	Functionality
Micro-controller	Controls the functionality of other components and processes the data
Transceiver	Transmits and receives signals
External Memory	Stores application related data
Battery	Source of energy

Wireless Sensor Network uses wireless communication for data transmission. As its transmission range is limited, a sensor node cannot transmit the sensed data directly to the base station. Hence sensor node transmits the data through multiple intermediate nodes in which routing protocols play a significant role.

Routing protocols in WSNs are broadly classified into two types based on network structure and protocol operation. Figure 1 shows further classification of network structure and protocol operation based routing protocols [1]. The routing protocols that were designed for WSNs were developed by keeping energy constraints in mind in order to prolong WSN lifetime, but security did not get its due share of consideration.

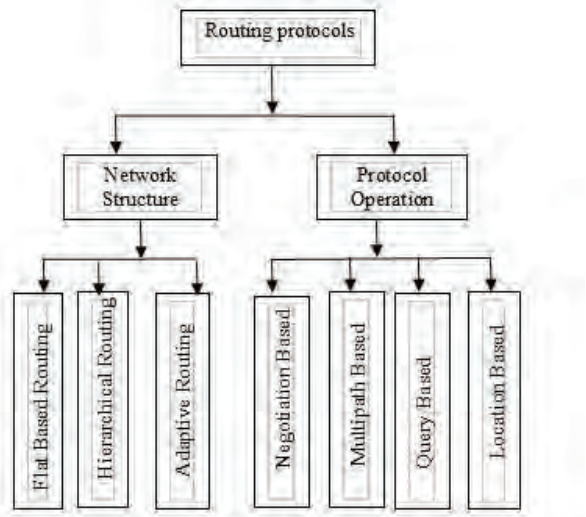

Figure 1. Classification of Routing Protocols in Wireless Sensor Networks

Routing protocols in Wireless Sensor Networks are exposed to various types of attacks. This paper discusses attacks and some of the defensive techniques reported in literature.

The paper is organized as follows: Various types of attacks on routing protocols are presented in detail in Section II. Defensive techniques for some of the attacks are discussed in Section III.

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Section II. Defensive techniques for some of the attacks are discussed in Section III.

II. Attacks on Routing Protocols

Nodes in WSN are vulnerable to physical attacks as the environment in which they are deployed is open, never or rarely attended and harsh and makes them susceptible to various types of attacks. Attacks in general can be external or internal. External attack on routing protocols aims at the following: introduce wrong routing information, replay old routing information, misinterpret the information resulting in partition or overload the network with increasing frequency of retransmission and also using inefficient routing. Internal attacks are highly detrimental and also not easily detectable. The following are different types of attacks on routing protocols in Wireless Sensor Networks:

- Spoofed/alter, replay routing information[8]
- Eavesdropping
- Hello Flood Attack[9]
- Selective Forwarding Attack[10]
- Sink Hole Attack[2]
- Worm Hole Attack[12]
- Sybil Attack[13]
- Acknowledgment Spoofing[14]
- Node Capture Attack

A. *Spoofed/alter/replay routing information*

In this attack an adversary passively captures the routing information that is being transmitted, spoofs/alters or replays the routing information which may create routing loops, convey false routing information, partition the network and so on.

B. *Eavesdropping*

This is an attack on the confidentiality of the data that is being transmitted. In this attack an adversary monitors the data without interrupting the normal operation of the network. An adversary can even launch traffic analysis by observing the traffic in the network.

C. *Hello Flood Attack*

In this attack, during the neighbor discovery phase an adversary transmits a "Hello" message with strong transmission power. The malicious node convinces the other nodes that the attacker is its neighbor, so all the nodes mark the attacker as its parent node. When the nodes in the network send data to the adversary, data is actually transmitted to the oblivion because the adversary is far away.

D. *Selective Forwarding Attack*

In selective forwarding a malicious node acts like a normal node, rejects to forward all the packets and selectively drops the packets carrying sensitive information.

Sensor node -

Malicious Node -

Base Station -

Packet -

Routing Path -

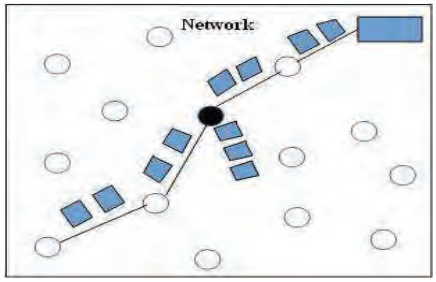

Figure 2. Illustration of Selective Forwarding Attack

E. *Sink Hole Attack*

With respect to routing metrics, a malicious node attracts its neighboring nodes and draws as much traffic as possible, and then the attacker may drop or modify the received packets or sometimes severe attacks like selective forwarding may be launched.

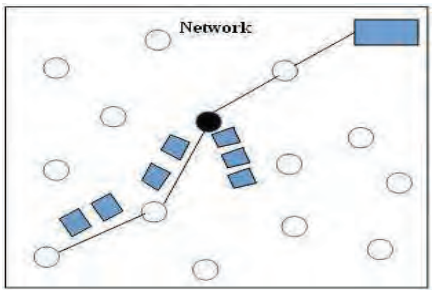

Figure 3. Illustration of Sink Hole Attack

F. *Worm Hole Attack*

In this attack two adversaries cooperate with each other, collect information at one location and replay from another location of the network.

G. *Sybil Attack*

In Sybil attack, a malicious node illegitimately claims multiple identities to represent multiple nodes in the network. In Figure 4 below, a malicious node claims different identities (A, B, C) with its neighbors.

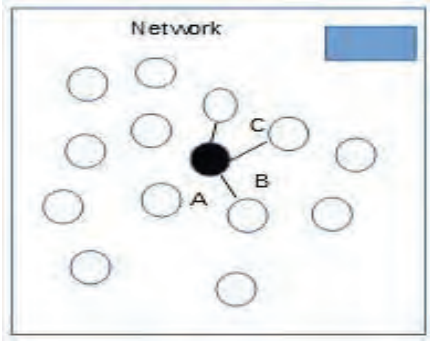

Figure 4. Illustration of Sybil attack

H. Acknowledgment Spoofing

In this attack, an adversary spoofs/forges the ACK packet. As a result, a weak link is assumed to be strong and a dead node as alive. Packets transmitted through these links may be lost or corrupted.

I. Node Capture Attack

As sensor networks are deployed in harsh and unattended environment, sensor nodes lack physical security. Hence an adversary may capture the sensor node and compromise not only sensitive data but also the key material used for security.

III. DEFENSIVE TECHNIQUES

This section discusses some of the defensive techniques proposed in literature to address the above mentioned attacks.

A. Selective Forwarding Attack

Selective Forwarding is an active and internal attack. In selective forwarding attack malicious nodes behaves like normal nodes but selectively drop data packets carrying sensitive data which destroy the entire monitoring system. Black hole is a special type of selective forwarding attack in which adversary rejects to forward all the packets. The defensive techniques proposed in literature for addressing selective forwarding attack are:

Multi Data flow Topologies

Multi Data Flow topologies (MDT) is one of the defensive techniques proposed in [3] to address selective forwarding attack. In the proposed MDT scheme before deployment the entire network is divided into different groups with overlapping regions. Each group belongs to one data flow topology. After deployment multi data flow topologies are built. Each node belongs to one data flow topologies and can communicate only with the nodes belonging to the same topology. If a malicious node belonging to one topology drops the packet, the base station still receives the dropped packets from other data flow topology because the monitoring area is overlapped. MDT scheme is simple and efficient, besides addressing selective forwarding attack it is also resistant to jamming attacks and there is no need to resend the dropped packets as the base station receives the dropped packets.

Yu and Xia [4] proposed a defensive scheme based on ACK packets. On the path of data transmission selected, intermediate nodes transmit ACK packets. With the ACK packets source node can easily identify the malicious nodes. The scheme is simple but the major drawback is the additional overhead associated with each node. Besides sensing and forwarding, the nodes must transmit ACK packets and are also responsible for identifying malicious nodes. The lost packets must be resent by the source node.

B. Worm Hole Attack

In worm hole attack two adversaries cooperate with each other, collect information at one location and replay from another location of the network. The defensive techniques proposed in the literature are:

Directional Antennas

Hu and Evas [5] proposed use of directional antennas to counter worm hole attack. In the proposed scheme every node is equipped with a directional antenna which examines the direction of received signal from the neighbor nodes with a shared witness. The relationship with the neighbors is confirmed only when the directions match. The main drawback in this scheme is that every node must be equipped with a special hardware component called directional antenna, which may not be a promising approach.

Packet Leashes

Hu et al. [6] proposed Packet Leashes for detecting and protecting the network from wormhole attack. Two types of packet leashes were proposed: geographic and temporal leashes. In case of geographic leashes geographic location of each node or a fixed clock synchronization between nodes is required. Geographic leash ensures that the packet travels up to a certain distance from the sender. In temporal leash every packet has a life time which strictly controls the maximum distance traveled by the packet. The drawbacks are either fixed clock synchronization between nodes and that information about the location of each node is required.

In [16] authors have presented an attack specific secure routing protocol specially designed to address worm hole attack. Neighbor discovery, initial route discovery, worm hole detection during data dissemination phase and finally discover a secure route against a worm hole attack are the four phases of this protocol.

C. Sybil Attack

In Sybil attack malicious node illegitimately claims multiple identities by stealing or fabricating identities of legitimate nodes. In [7] various defensive techniques to address Sybil attack are proposed.

Random Key Pre-Distribution

In literature researchers have proposed many random key pre-distribution schemes to establish secure links between the nodes. By using key distribution schemes Sybil attack can be addressed.

Position Verification

Another defensive technique to prevent Sybil attack is position verification. In this approach the network identifies the physical location of each node, with which malicious nodes claiming multiple identities can be identified. But automatic location detection is still an open research problem. This solution suits static networks rather than dynamic networks or networks with mobile nodes.

Code Attestation

The code running on a malicious node must be different from that of the code running on legitimate node.

By verifying the memory content i.e. the code, malicious nodes can be easily identified. But this approach is expensive.

Registration

By registering the identities of the sensor nodes in the network to the trusted central authority (i.e the base station) sensor networks can prevent Sybil nodes. But the drawback is that the list of registered nodes and the deployment information must be securely maintained and protected from being maliciously modified.

D. Sink Hole

Sink hole is an internal attack in which a malicious node convinces the neighboring nodes by advertising single-hop, high quality path to the destination and attracts the traffic as much as possible, and the packets destined to the base station are dropped or modified by the sink hole node.

In [12] authors have proposed an attack-specific secure routing protocol. The proposed protocol uses redundancy based mechanism to address sink hole attack. In this protocol the messages are sent to the suspicious nodes through multiple paths, the attacked nodes are confirmed by evaluating the replies comprehensively.

E. Eavesdropping

Eavesdropping is a passive attack in which the adversary just monitors the data being transmitted between the source and destination without disturbing the normal operation. The countermeasure is encryption. But choosing a light weight and strong encryption algorithm is a challenging task in Wireless Sensor Networks because of the limited resources. Many secure routing protocols are proposed in literature [13, 14, 15]. The protocols provide confidentiality for the data that is being transmitted and protect the data from eavesdropping.

F. Replay

Replay is an active attack in which the adversary passively captures data or the routing information and subsequently replays it to create an unauthorized effect. The counter measure is to include a field in the packet so that the packet can be uniquely identified, like sequence number or time stamp or a nonce.

TABLE II

Summary of Attacks and Countermeasures

ATTACKS	COUNTERMEASURES
Eavesdropping	Encryption
Selective Forwarding	Multi Data flow Topologies, Acknowledgment
Worm Hole Attack	Directional Antennas, Packet Leashes, Authentication
Sybil Attack	Authentication, Random Pre-key distribution, Position verification, Code attestation, Registration
Sink Hole Attack	Authentication, Redundancy based mechanism
Hello Flood Attack	Authentication

IV. CONCLUSIONS

In this paper security issues relating to the routing protocols in Wireless Sensor Networks have been discussed in detail. Defensive techniques proposed in literature have been presented. Based on the survey it is found that there is a need to design a secure routing protocol which can provide basic security services like confidentiality, authentication, integrity and availability, addressing all the known types of attacks.

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Impact of Green Marketing on Green Consumer Behaviour

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***Abstract*—Green marketing is increasing globally and is influencing consumer's purchasing behaviour. Firms have started responding to environmental challenges by practicing Green Marketing strategies. Environmental Concern has become an important topic in research. The main objective of this study is to measure the impact of green marketing strategies on consumer buying behaviour. The results demonstrated that green product, green advertising, green packaging and ecolabel have significant impact on consumer buying behaviour.**

***Index Terms*—Green Product, Green Packaging, EcoLabel, Green Advertising, Green Consumer Behaviour**

I. INTRODUCTION

Green Marketing is designing, promoting, pricing and distributing products in a manner which promotes environmental protection and which is less detrimental to the environment. (Polonsky, 2011). Firms are adopting green marketing as a social and moral responsibility, to be more competitive, for customer satisfaction and to expand their market. Environmental awareness and concern for environment have an influence on the consumer buying behaviour. Consumers are shifting to green products to make a positive impact on the environment. Green purchase behaviour is also influenced by other factors such as social, cultural and demographic factors (Yatish Joshi, et.al, 2015). Consumers evaluate various social, environmental and individual consequences while purchasing a green product.Government regulation related to Green Marketing also help in reducing the production and consumption of harmful products.

II. LITERATURE REVIEW

Implementation of green marketing strategies requires huge investment in technology, and Reasearch and Development. But green marketing strategies such as ecodesign of a product, ecolabel, ecopackaging and green logo are required to face stiff competition and to have a positive impact on the customers and on the environment (Manjunath.G, 2013). Consumers want high quality products that are environmentally safe (D'Souza, et.al., 2006). Green Corporate perception and green product value have significant influence on green purchase intention. Firms should ensure that environmental performances of their product are in accordance with customer perceived value of the green product (Collins Marfo Agyeman,(2014). Though environmental advertisement has a positive effect on consumer purchasing behaviour, an increased awareness on ecolabels would help in promoting green product consumption among consumers (Narges Delafrooz,et.al., 2014).The marketers have to focus on the demographic profile of their consumers. Most of the marketers do not consider it important while formulating green marketing strategies. But the differences in age, income, gender and literacy create a huge difference for implementation of green marketing strategies (Meghna Sharma, et.al., 2016). The designing of the green products such as packaging, labeling and quality should be in congruence with the eco concepts so that customers can associate the green products with an appropriate image (Charlie, et.al., 2014). Green marketing presents challenges because of the absence of clear understanding of the cause and effect relationships in matters affecting the environment. Since green marketing is sustainable marketing, networking resources and implementing a green strategy will be perilous (Mohammad Jalalkamali, et.al., 2016). Green perceived value has a positive influence on trust and purchase intention of the customers. Resources have to be invested in increasing the green perceived value (Chen and Chang, 2012). To cope up with health issues, climatic changes, environmental legalizations and government policies and to enhance the goodwill of the firm, it is essential to implement green marketing strategies. (Babita Saini, 2013).

III. OBJECTIVES OF STUDY

The main objective of the study is to measure the impact of green marketing strategies on green consumer buying behaviour. For this purpose, four green marketing strategies such as green product, green packaging, ecolabel and green advertisement were considered in this study.

IV. RESEARCH METHODOLOGY

This study is based on the survey conducted in Hyderabad (Telangana) during June 2015-February 2016.The theoretical foundation of the study is based on various secondary sources such as texts on articles, magazines, published papers. The primary data was collected using Judgment (Purposive) sampling. The respondents were selected on the basis of judgment to include all demographic segments. The theoretical foundation of the study is based on various secondary sources such as texts on articles, magazines, published

papers. The structured questionnaire is used to get the responses of the respondents. For the purpose of primary data collection, data were collected from 250 respondents of Hyderabad but only 219 responses came out to be relevant to the study. The data for this study were collected through the distribution of self administered questionnaires via online method (email) and offline method (hand delivery) to potential respondents across Hyderabad. The respondents were asked to express their agreement or disagreement with a statement on a fivepoint Likert type scale (1 = strongly disagree, 2 = disagree, 3 = neutral, 4 = agree, 5 = strongly agree). The statistical package for the Social Sciences Program (SPSS) was used in the study for statistical data analysis. Factor analysis is carried out by the researcher. A frequency distribution is used to describe the sample. For the purpose of the present study, descriptive research design and quantitative research method are used.

V. Data Analysis and Data Interpretation

TABLE I

DEMOGRAPHIC FACTORS OF RESPONDENTS

Demographic Factors	No. of Respondents	Percentage
Age		
20-30 years	58	26
30-40 years	67	31
41-50 years	54	25
Above 50 years	40	18
Gender		
Male	95	43
Female	124	57
Marital Status		
Single	82	37
Married	137	63
Profession		
Services	80	36
Businessmen	74	34
Housewife	65	30
Annual Income(Rs)		
3,00,000-5,00,000	49	22
5,00,001-7,00,000	73	33
7,00,001-9,00,000	69	32
More than 9,00,000	28	13

TABLE II

FACTOR LOADINGS FOR GREEN PRODUCT VARIABLES

Green Product	Loadings
Recyclable	0.754
Energy Efficient	0.788
Made with recycled content	0.710
Biodegradable	0.665
Reusable	0.683
Organic	0.796
Use of renewable resources in production process	0.628

The table above shows that there are positive loadings on all the green product variables. Recyclable, energy efficient, biodegradable, reusable, organic, made with recycled content, and which uses renewable resources in the production process have significant influence on green consumer behaviour. Green Product has emerged as a separate factor with an eigen value of 2.79.The above table shows that Green Product variable 'Organic', has got the highest loading of 0.796.

TABLE III

FACTOR LOADING FOR GREEN PACKAGING VARIABLES

Green Packaging	Loadings
Use of minimal materials	0.648
Energy efficient	0.730
Made with Recycled content	0.657
recyclability	0.777
Reusable packaging	0.762
Use of renewable resources in packaging	0.591
Made with Biodegradable and compostable materials	0.785

The table above shows that there are positive loadings on all the green packaging variables. Energy efficient, recyclable, reusable, made with recycled content, renewable and which is made with Biodegradable and compostable materials have significant influence on green consumer behaviour. Green Packaging with an eigen value of 2.65 has also been identified as one of the important influencing factors on Green Consumer Behaviour. The above table shows that Green Packaging variable 'Made with Biodegradable and compostable materials', has got the highest loading of 0.785.

TABLE IV

FACTOR LOADINGS FOR ECO LABEL VARIABLES

Eco Label	Loadings
Informative	0.779
Trust-worthy	0.716
Helps in making purchasing decisions	0.742
Provides authenticity	0.735

The table above shows that there are positive loadings on all the Eco Label variables. Informative, trustworthy, authentic and which helps in making purchasing decisions have significant influence on the green consumer behaviour. EcoLabel has been identified as a separate factor with an eigen value of 2.71.The above table shows that the Eco Label variable 'Informative', has got the highest loading of 0.779.

TABLE V

FACTOR LOADINGS FOR GREEN ADVERTISING VARIABLES

Green Advertising	Loadings
Informative	0.725
Boosts confidence	0.648
Reflects brand's environmental efforts	0.690
Motivates pro-environmental attitudes	0.703

The table above shows that there are positive loadings on all the Green Advertising variables. Informative, boost confidence, reflecting brand's environmental efforts and which motivates pro-environmental attitudes have significant influence on the green consumer behaviour. Green Advertising has been identified as separate factor with eigen value of 2.53. The above table shows that the Green Advertising variable ‘Informative’ has got the highest loading of 0.724.

TABLE VI
FACTOR LOADINGS FOR GREEN CONSUMER BEHAVIOUR VARIABLES

Green Consumer Behaviour	Loadings
Environmental concern	0.819
Environmental responsibility	0.771
More Efforts to buy green products	0.738
Gather information about green products	0.799
Willing to pay high price for green products	0.683
Recommend green products to others	0.614
Willingness to pay an environmental tax	0.607
Strong supporter of environmental regulation	0.811

The table above shows that there are positive loadings on all the Green Consumer Behaviour variables. Green Consumer Behaviour has been identified as a separate factor with an eigen value of 2.82. The table above shows that the Green Advertising variable 'Informative' has got the highest loading of 0.724.

VI . CONCLUSIONS

A company can enhance its brand image and secure its market share among the growing number of environmentally concerned consumers by adding Green Marketing to its business strategy. Green Consumers make purchase decisions based on the information about the product and the manufacturer rather than on attractive advertising campaign. Green consumers want to know the potential impact of the product on the environment after usage.

Green Consumers are giving preference to organic and energy efficient products. They consider it as their environmental responsibility to buy recyclable products. Consumers' choice for green products is influenced by the packaging too. They prefer recyclable and reusable packaging. The green consumers have to be supplied with details and authenticity on their Green claims. Though the Green consumers have environmental concern, they may not be willing to pay higher price for the green products.

Therefore the producers should not neglect the traditional consumer values of reasonable price and high quality, despite the exciting opportunities of the green consumer market.

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Puerilism in the novel, Waiting for the Mahatma

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Abstract: **"Waiting for the Mahatma", is a more distinct novel than that of other novels written by R.K.Narayan. He depicts an Indian culture predominantly, a South Indian village life. His characters are alive through his description; his settings are vibrant and are reproduced in his pictorial descriptions. The research paper studies how R.K.Narayan depicted the protagonist's character in this novel. In several situations in the novel the protagonist, Sriram behaves like an infant. The infantile behaviour in adulthood is called Puerilism. In this paper a few situations have been taken and analysed to reveal Sriram's character which depicts puerilistic behaviour. This is judged based on the observation of cultural and sociological impact upon a person. We study how family and cultural circumstances impact Sriram.**

Key words: **Distinct, Depict, Predominantly, Puerilism, Vibrant**

I. AIMS AND OBJECTIVES OF THE RESEARCH PAPER:

1. The aim of the research paper is to demonstrate how the protagonist's character has been portrayed by R.K.Narayan in puerilistic way.
2. Some people in the society behave like children even in adulthood because of their background.
3. A term in psychology Puerilism has been chosen as a key word because it means infantile behaviour in adulthood and the term has been applied to Sriram's character.

I. INTRODUCTION

Puerilism is the attitude of a person whose behaviour is juvenile in adulthood. It is based on the influence of apparent cultural and sociological facts. We shall not connect any psychological implications to it. If possible, everyone would behave in calm, rational, balanced manner in different situations. But unfortunately, some people just never grow up completely. If they have to deal with people, they don't keep their sanity. Some people are attention junkies who want all eyes and ears focused on them. Some people are always whining about something. Some people are totally dependent on family members for decision making.

Sometimes adults argue about the things that they are passionate about. This can result in their reminiscences about how they were thinking during their childhood. It can bring out an aspect of such person that is immature, since they want to appear to be correct and want to "win" every argument. People sometimes argue with others because they feel, they have to prove their point. They want that kind of approval and respect, and they think, they will earn it by arguing until they get their way.

II. REASONS FOR PUERILISTIC BEHAVIOUR

Most adults build up all their anger, opinions and stress because they consider that they require it. They don't share their problems often and as obstinate as they are, they often think that they don't need to give evidence for anything. A lot of parents have "do as I say" instead of "do as I do" attitude. They expect their children to jump through hoops without any question simply because he is their child. If not, they throw childish fits because they are afraid of losing control. A lot of adults don't appear to comprehend how they do something though and often don't want to listen to either.

Occasionally the squabble isn't really about the trivial things. Sometimes it is about something greater and one or both of the adults don't have healthy ways of resolving conflicts and tensions so they end up fighting like toddlers over little things also. The big things may be hard to talk about. Both have to focus and work on to resolve it.

Undeveloped adults are hardly ever bad, stupid neither lazy, nor are they immature all the time. Immature adult behaviour reflects a lack of mature parenting and other childhood disappointments. The consequences are most apparent in adults' behaviour. The results of immature parenting include adults who act childishly, driven by obnoxious emotions, obsessions, compulsions and fixations. They may incessantly repeat whatever they did as children to get some alternative for parental love.

Their childlike behaviour may prevent them from considering how their behaviour affects other people. Immature adults frequently observe other people as possible sources for their childish needs, not as human beings who have needs and feelings of their own. Things become more complicated if one ignores the actual age of a person inspite of the childish behaviour and hopes that he will somehow grow up. If one learns to recognize what causes and maintains their childish or teenage behaviour, one can better communicate with them.

Occasionally they can't act like responsible adults. At times they are children mentally and emotionally. One shouldn't be misled by their physical age, education or intelligence - childish people often forget what they have learnt during their childhood. One should try to guess their emotional age. Notice when one acts childishly or feels like a teenager, and gain insight into immaturity. Common triggers for age regression include pain, certain places, certain voices; tricky memories or music that was liked by him as a teenager of their age and background. They may

express their desires without being. They may have a little idea of who they are although they always know what they need. Not only are they perplexed about who they are, they are perplexed about who you are. And if one allows oneself to become entangled with them, they may be just perplexed.

III. SOLUTIONS

On occasions when we know of their childishness; we can treat those people like children. We can give details of their limits, make contingency plans, reward adequate behaviour and describe what is not adequate and the consequences of their violations. Approximately one in every four people might experience an emotional or relationship catastrophe. Perhaps blame may be on economic reasons, on a partner or on some other conflict. Many of these people will seem to shut down, become depressed and express age-regressed emotions. They act childishly and to make childish threats.

Nevertheless, immature people who want to feel good without effort may resent any hints that their behaviour is at fault. One shouldn't expect to be showered in appreciation if they mention that their mental status is late for a wash. Childhood disturbance can lead to an incapability to make adult decisions; with coupled associated embarrassment, guilt and self-abuse, as well as limiting beliefs, learning disabilities, depression and relationship disorder. We can help them locate and incorporate their childish parts as steps on their trail to emotional maturity and adult relationships.

IV. A FEW SITUATIONS IN THE NOVEL WHICH REVEAL SRIRAM'S PUERILISTIC BEHAVIOUR

The protagonist, Sriram's character has been depicted in a puerilistic way. His mother died immediately after he was born and his father was killed in Mesopotamian war. He was brought up by his grandmother. When postman brings oblong cover on the first day of every month, addressed to his grandmother, she weeps on seeing it; his infantile behaviour makes him wonder. When he was about one year old, his grandmother used to show the traffic passing outside, making him sit on the cold cement window-sill. Thus sitting on window-sill becomes a habit for him. When he grows up, he seeks no other place except the window-sill. His grandmother reproaches him for not mingling with the others of his age, he replies that he feels happy being alone. Thus he becomes an introvert and adapts to only that kind of environment. He behaves like a child in several situations in the novel.

On the twentieth birth day of Sriram, his grandmother decorates the house with mango leaves and she brings sugar-cane, as she feels bringing sugar-cane is very auspicious. She wants to call neighbours to celebrate his birthday grandly, but her solitary grandson prohibits her from inviting anyone. She has been planning to celebrate his twentieth birthday, engaging pipes and drums and processions for the particular birthday to hand over the savings pass book to him and give up the trust. All her plans have become futile because of his behaviour. When she takes him to the bank to open an independent account, the neighbours call him an urchin, she shouts at them, saying he is not an urchin and says he is old enough to take charge of his own affairs.

In one instance in the novel, Sriram meets a young lady, Bharathi who is a follower of Gandhiji at their camp. She is very talkative and sharp-tongued girl. He wants to be a volunteer of Gandhiji's camp for being in her company. He feels that Bharathi is a very good match for him. When he keeps on asking questions to infatuate her, she gets irritated. She doesn't answer him properly. He uses malapropisms while answering; she easily notices that he has turned up for her. After knowing that he is a parentless man who is brought up by his grandmother, she becomes tender and speaks to him kindly. After the conversation he realises that it is difficult to please her and knows that she is a termagant. He gets to know that she is a parentless girl like him. He convinces her saying he has something to do without wasting time in life. He pleads with her to allow him as one of Gandhiji's disciples. She asks him what he would tell his grandmother. Then he mumbles and makes some indistinct sounds. He also asks her what he has to do. On hearing this she feels that she is superior to him in intelligence and questions why she should talk to him. He says that he likes her and wants to be with her. Then she bursts into laughter and says, "That won't be sufficient". If you speak like that, they may chase you away. He becomes sullen and gloomy. She enjoys teasing him. Now he really wants to do something and tells her not to make fun of him. She asks him whether he would be willing to meet her. He replies that he is not interested in meeting and tells her that he doesn't know how to behave with her. She becomes very serious with him and commands that he must face Gandhiji if he really wants to work with him. Then he loses his temper and cries at Bharathi that he would meet her anywhere except before Gandhiji. He doesn't want to become a fool before Gandhiji. Bharathi replies finally if he wishes to meet her, the only place he could meet her was before Gandhiji. If he doesn't want to meet her there, he can leave her. Sriram agrees to meet her there at 3.00am.

Sriram has been given a task of spreading the message of Quit India by writing "Quit India" on far-flung villages of the area. He travels in the forest area where elephants were hauling timber. The timber contractor exports the timber to far off countries for money. He explains the contractor that the British are going to use this timber for the destruction of the world by making ships and rifles. The timber contractor pleads with him not to trouble them and informs that they are just business men. Then Sriram tells him that this is not the time for acquiring money but time to join in the fight for independence. Sriram informs him about Gandhiji's non-violence, but he is not convinced with the message, as he is interested in making money. The contractor treats him like a child. Sriram knows that it is difficult to convince him. He can't understand that he is treated like a child. He decides to leave the contractor and goes to other villages from there.

In Solur village Sriram has a funny conversation with the shopkeeper. The shop keeper asks where he is from, he replies, "from faraway" and he enquires where he is going and he replies, "Faraway" again. The people at the shop laugh at this. The shopkeeper asks him to have nice biscuits. Sriram asks whether they are from England. Then he replies yes and says that he got them from his friend who is in the army. Sriram scolds him for selling biscuits from England. The shopkeeper calls him a rowdy and ridicules him for the khadi dresses. He is hurt by such comments. Sriram threatens the shopkeeper that he can talk anything about him, but not about the dress, as it is too scared to be spoken in that way. The shop keeper feels intimidated by his manner. Sriram wants to make him understand the importance of the dress and not selling foreign goods. The shop keeper doesn't want the little circle of watchful people who are gathering. But Sriram does not leave him and sits in front of the shop. He there behaves like a child who is sulky with his mother for not giving him money. The people enjoy the scene. He doesn't even allow customers to buy anything in the shop until the shop man throws biscuits into the drain. The shop man apologises and assures him that he won't sell foreign goods again. This pleases Sriram and he leaves from there.

A person, Jagadish comes across Sriram one day and introduces himself as a national worker. He also says that one of his friends met Bharathi in the jail. This makes Sriram happy and enquires about Bharathi. Jagadish easily swindles him saying that he is a follower of Gandhiji's non-violence. Gradually he becomes closer to Jagadish and involves in his violent activities, though he has trepidation. He sets fire to the court records in different places, derails couple of trains and explodes bombs. Sriram once questions Jagadish about violent activities and loss of people's lives. Jagadish convinces him. But he is not sure if this is right or wrong. He recollects Bharathi if she is with him she would have helped. Then the police search for Sriram because of his violent activities. He is arrested by the police, when he saves the grandmother from the pyre. This shows how he is treated as gullible by the other characters in the novel.

V. CONCLUSIONS

This research paper studies a few reasons and solutions for puerilistic attitude. The protagonist, Sriram's conversation with his grandmother, Bharathi, the timber contractor, shopkeeper in Solur village, and Jadish has been presented in the paper. Thus the few situations in the novel reveal that Sriram's character has puerilistic attitude because of social and cultural impacts on him.

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1. Waiting for Mahatma, Indian thought Publications.
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Template for the Preparation of Papers for Publication in In-house Journal of CVR College

First A. Author[1] and Second B. Author[2]
[1] Name of Institution/Department, City, Country
Email: first.author@hostname1.org
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***Abstract*—These instructions give you basic guidelines for preparing camera-ready papers for CVR College journal Publications. Your cooperation in this matter will help in producing a high quality journal.**

***Index Terms*—first term, second term, third term, fourth term, fifth term, sixth term**

I. Introduction

Your goal is to simulate the usual appearance of papers in a Journal Publication of the CVR College. We are requesting that you follow these guidelines as closely as possible.

A. Full-Sized Camera-Ready (CR) Copy

Prepare your CR paper in full-size format, on A4 paper (210 x 297 mm, 8.27 x 11.69 in). No header or footer, no page number.

Type sizes and typefaces: Follow the type sizes specified in Table I. As an aid in gauging type size, 1 point is about 0.35 mm. The size of the lowercase letter "j" will give the point size. Times New Roman has to be the font for main text. Paper should be single spaced.

Margins: top = 30mm (1.18 in), bottom, left and right = 20 mm (0.79 in). The column width is 82mm (3.23 in). The space between the two columns is 6mm (0.24 in). Paragraph indentation is 3.7 mm (0.15 in).

Left- and right-justify your columns. Use tables and figures to adjust column length. On the last page of your paper, adjust the lengths of the columns so that they are equal. Use automatic hyphenation and check spelling. Digitize or paste down figures.

For the Title use 24-point Times New Roman font, an initial capital letter for each word. Its paragraph description should be set so that the line spacing is single with 6-point spacing before and 6-point spacing after. Use two additional line spacings of 10 points before the beginning of the double column section, as shown above.

Each major section begins with a Heading in 10 point Times New Roman font centered within the column and numbered using Roman numerals (except for ACKNOWLEDGEMENT and REFERENCES), followed by a period, two spaces, and the title using an initial capital letter for each word. The remaining letters are in SMALL CAPITALS (8 point). The paragraph description of the section heading line should be set for 12 points before and 6 points after.

TABLE I.
TYPE SIZES FOR CAMERA-READY PAPERS

Type size (pts.)	Appearance		
	Regular	Bold	Italic
6	Table caption, table superscripts		
8	Section titles, tables, table names, first letters in table captions, figure captions, footnotes, text subscripts, and superscripts		
9	References, authors' biographies	Abstract	
10	Authors' affiliations, main text, equations, first letters in section titles		Subheading
11	Authors' names		
24	Paper title		

Subheadings should be 10 point, italic, left justified, and numbered with letters (A, B, …), followed by a period, two spaces, and the title using an initial capital letter for each word. The paragraph description of the subheading line should be set for 6 points before and 3 points after.

For main text, paragraph spacing should be single spaced, no space between paragraphs. Paragraph indentation should be 3.7mm/0.21in, but no indentation for abstract & index terms.

II. Helpful Hints

A. Figures and Tables

Position figures and tables at the tops and bottoms of columns. Avoid placing them in the middle of columns. Large figures and tables may span across both columns. Leave sufficient room between the figures/tables and the main text. Figure captions should be centered below the figures; table captions should be centered above. Avoid placing figures and tables before their first mention in the text. Use the abbreviation "Fig. 1," even at the beginning of a sentence.

To figure axis labels, use words rather than symbols. Do not label axes only with units. Do not label axes with

Footnotes: 8-point Times New Roman font; copyright credit, project number, corresponding author, etc.

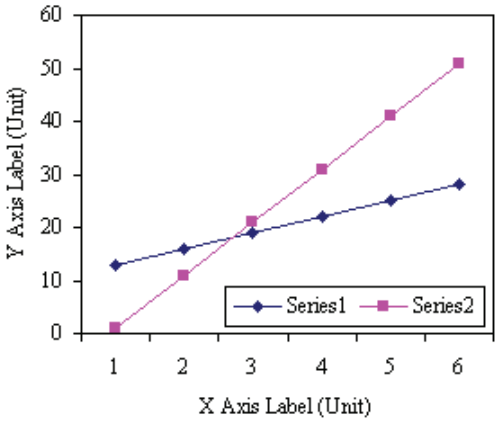

Figure 2. Note how the caption is centered in the column.

a ratio of quantities and units. Figure labels should be legible, about 9-point type.

Color figures will be appearing only in online publication. All figures will be black and white graphs in print publication.

B. References

Number citations consecutively in square brackets [1]. Punctuation follows the bracket [2]. Use "Ref. [3]" or "Reference [3]" at the beginning of a sentence:

Give all authors' names; use "et al." if there are six authors or more. Papers that have not been published, even if they have been submitted for publication, should be cited as "unpublished" [4]. Papers that have been accepted for publication should be cited as "in press" [5]. In a paper title, capitalize the first word and all other words except for conjunctions, prepositions less than seven letters, and prepositional phrases.

C. Footnotes

Number footnotes separately in superscripts [1, 2, …]. Place the actual footnote at the bottom of the column in which it was cited, as in this column. See first page footnote as an example.

D. Abbreviations and Acronyms

Define abbreviations and acronyms the first time they are used in the text, even after they have been defined in the abstract. Do not use abbreviations in the title unless they are unavoidable.

E. Equations

Equations should be left justified in the column. The paragraph description of the line containing the equation should be set for 6 points before and 6 points after. Number equations consecutively with equation numbers in parentheses flush with the right margin, as in (1). Italicize Roman symbols for quantities and variables, but not Greek symbols. Punctuate equations with commas or periods when they are part of a sentence, as in

$$a + b = c \ . \tag{1}$$

Symbols in your equation should be defined before the equation appears or immediately following. Use "(1)," not "Eq. (1)" or "equation (1)," except at the beginning of a sentence: "Equation (1) is ..."

F. Other Recommendations

Use either SI (MKS) or CGS as primary units. (SI units are encouraged.) If your native language is not English, try to get a native English-speaking colleague to proofread your paper. Do not add page numbers.

CONCLUSIONS

The authors can conclude on the topic discussed and proposed. Future enhancement can also be briefed here.

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The College has been given Permanent Affiliation by JNTUH and is accredited by NAAC with 'A' grade and also by National Board of Accreditation (NBA). It has also been accorded AAA+ status by Careers360 on par with decades old institutions in the states of Telangana and Andhra Pradesh. In keeping with the current global emphasis on green and eco-friendly energy generation, 280kW Solar PV plant has been installed in the campus to meet the power requirements of the college to a significant extent.

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